



STD55NH2LL STD55NH2LL-1

N-channel 24V - 0.010Ω - 40A - DPAK/IPAK
 Ultra low gate charge STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STD55NH2LL-1	24V	<0.011Ω	40A ⁽¹⁾
STD55NH2LL	24V	<0.011Ω	40A ⁽¹⁾

1. Value limited by wire bonding

- R_{DS(ON)} * Qg industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

Description

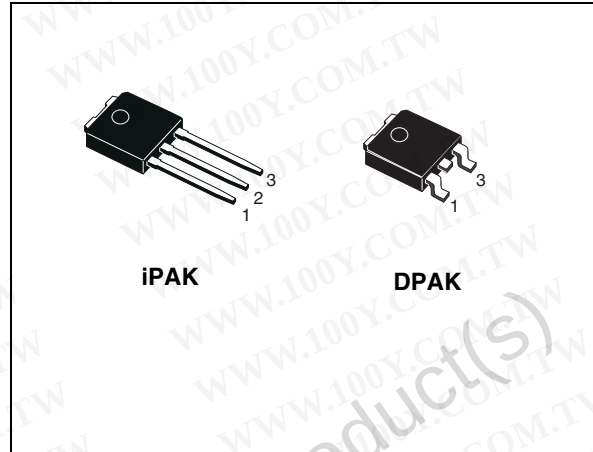
The STD55NH2LL is based on the latest generation of ST's proprietary STripFET™ technology. An innovative layout enables the device to also exhibit extremely low gate charge for the most demanding requirements as high-side switch in high-frequency DC-DC converters. It's therefore ideal for high-density converters in Telecom and Computer applications.

Applications

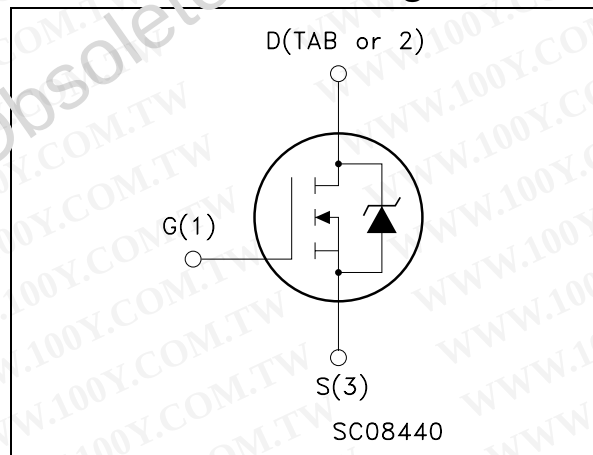
- Switching application

Order codes

Part number	Marking	Package	Packaging
STD55NH2LL-1	D55NH2LL	IPAK	Tube
STD55NH2LLT4	D55NH2LL	DPAK	Tape & reel



Internal schematic diagram



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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{\text{spike}}^{(1)}$	Drain-source voltage rating	30	V
V_{DS}	Drain-source voltage ($V_{\text{GS}} = 0$)	24	V
V_{DGR}	Drain-gate voltage ($R_{\text{GS}} = 20 \text{ k}\Omega$)	24	V
V_{GS}	Gate- source voltage	± 16	V
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$	40	A
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}} = 100^{\circ}\text{C}$	28	A
$I_{\text{DM}}^{(3)}$	Drain current (pulsed)	160	A
P_{tot}	Total dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$	60	W
	Derating Factor	0.4	W/ $^{\circ}\text{C}$
$E_{\text{AS}}^{(4)}$	Single pulse avalanche energy	600	mJ
T_{stg}	Storage temperature	-55 to 175	$^{\circ}\text{C}$
T_{j}	Max. operating junction temperature		

1. Garanted when external $R_{\text{g}}=4.7 \text{ }\Omega$ and $t_{\text{f}} < t_{\text{fmax}}$.

2. Value limited by wire bonding

3. Pulse width limited by safe operating area.

4. Starting $T_{\text{j}} = 25^{\circ}\text{C}$, $I_{\text{D}} = 20\text{A}$, $V_{\text{DD}} = 15\text{V}$

Table 2. Thermal data

$R_{\text{thj-case}}$	Thermal resistance junction-case max	2.5	$^{\circ}\text{C/W}$
$R_{\text{thj-amb}}$	Thermal resistance junction-ambient max	100	$^{\circ}\text{C/W}$
T_{j}	Maximum lead temperature for soldering purpose	275	$^{\circ}\text{C}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 25\text{mA}$, $V_{GS} = 0$	24			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$ $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 20\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 20\text{A}$		0.010 0.012	0.011 0.0135	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10\text{V}$, $I_D = 10\text{A}$		18		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		990 385 40		pF pF pF
R_G	Gate Input Resistance	$f = 1\text{MHz}$ Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1.3		Ω
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 10\text{V}$, $I_D = 20\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{V}$ (see Figure 13)		15 56 13 10		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$0.44\text{V} \leq V_{DD} \leq 10\text{V}$, $I_D = 40\text{A}$, $V_{GS} = 4.5\text{V}$, $R_G = 4.7\Omega$ (see Figure 14)		8.7 4.2 2.4	11	nC nC nC
$Q_{oss}^{(2)}$	Output charge	$V_{DS} = 16\text{V}$, $V_{GS} = 0\text{V}$		7.6		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. $Q_{oss} = C_{oss} \cdot \Delta V_{in}$, $C_{oss} = C_{gd} + C_{ds}$. See [Chapter 4: Appendix A](#)

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				40	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				160	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20A, V_{GS} = 0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 40A, di/dt = 100A/\mu s,$		32.5		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 15V, T_J = 150^\circ C$		28		nC
I_{RRM}	Reverse recovery current	(see Figure 15)		1.7		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

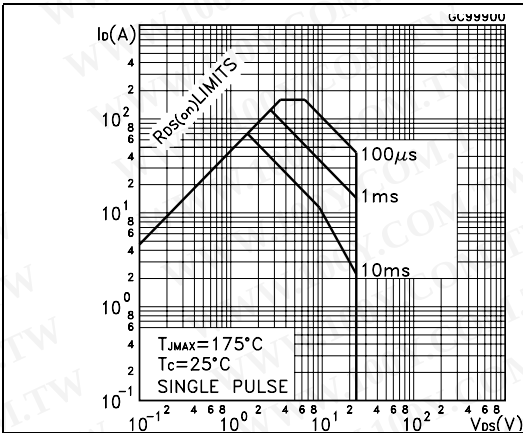


Figure 2. Thermal impedance

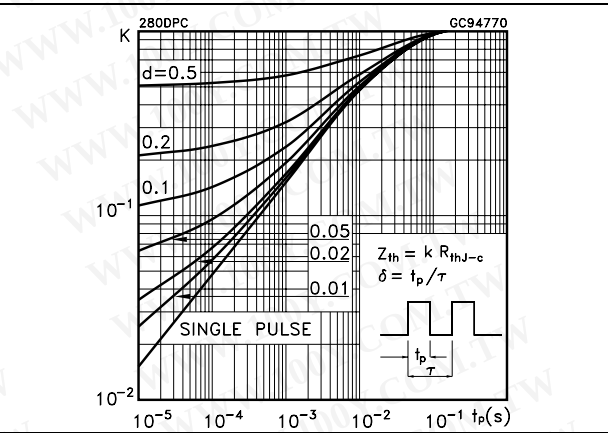


Figure 3. Output characteristics

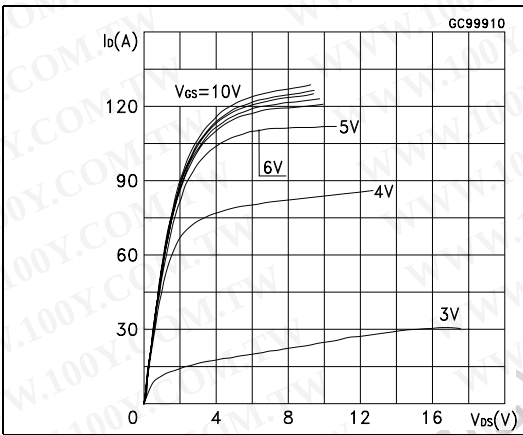


Figure 4. Transfer characteristics

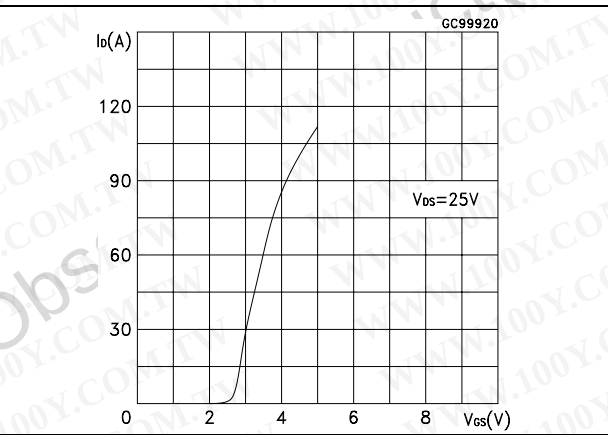


Figure 5. Transconductance

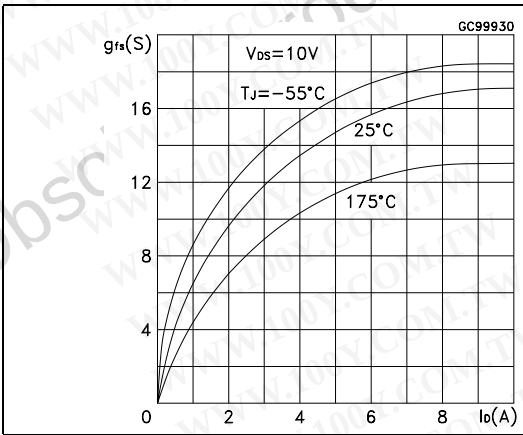


Figure 6. Static drain-source on resistance

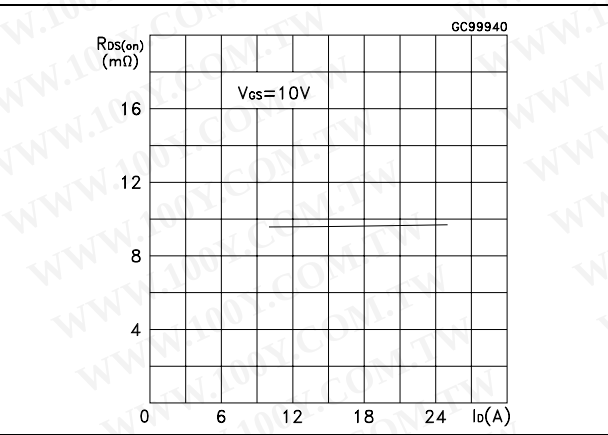


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

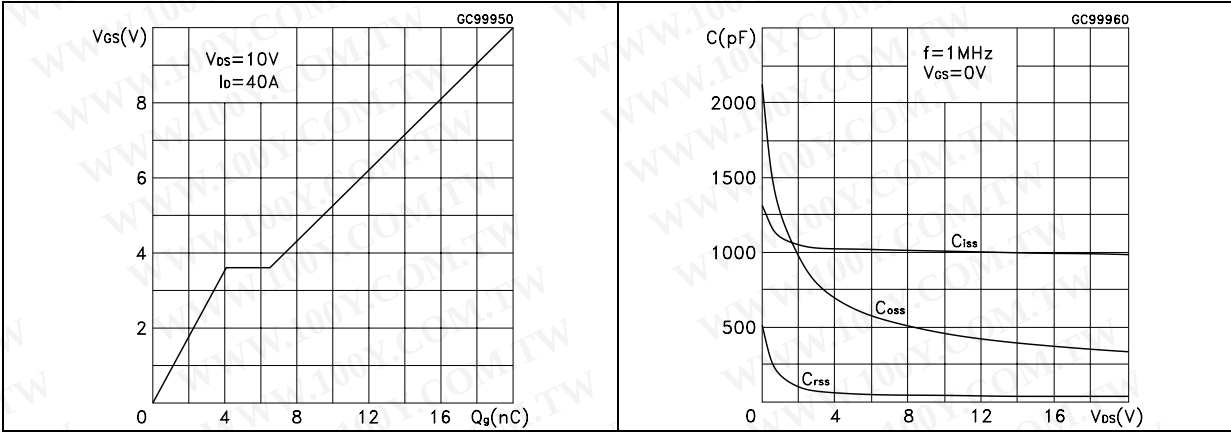


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

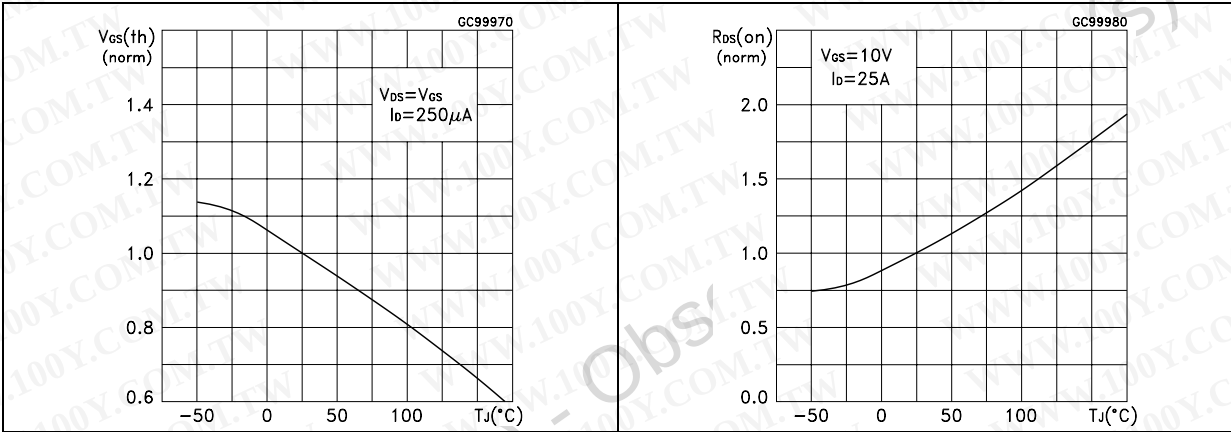
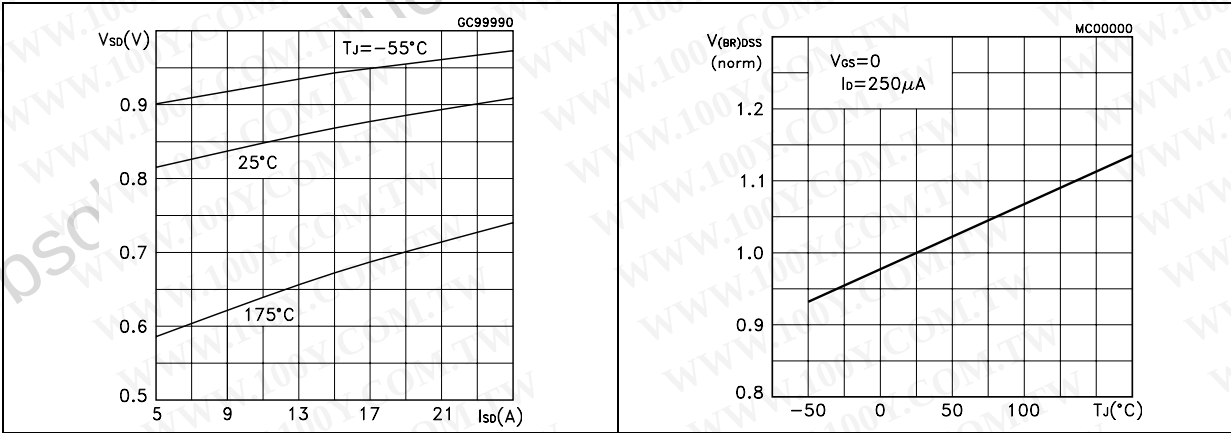


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

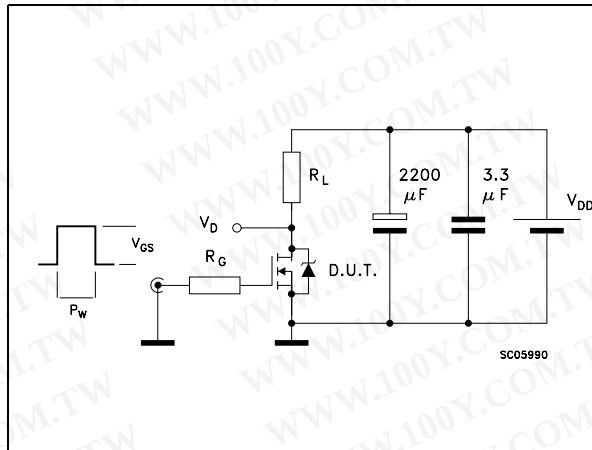


Figure 14. Gate charge test circuit

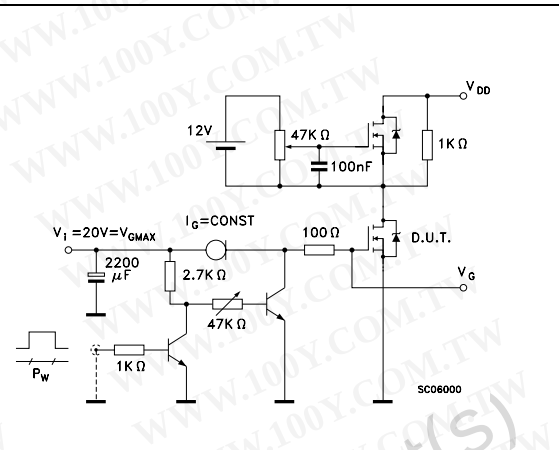


Figure 15. Test circuit for inductive load switching and diode recovery times

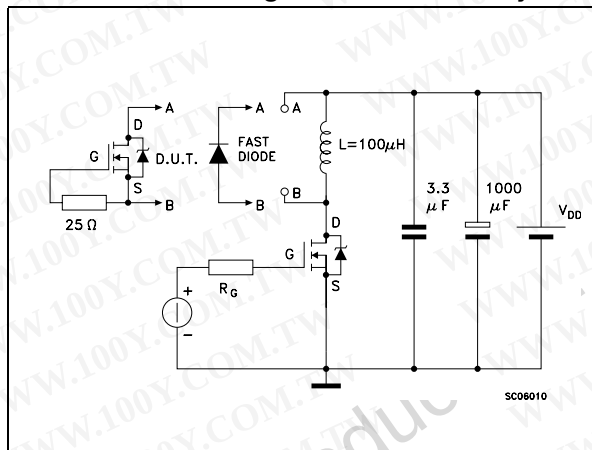


Figure 16. Unclamped Inductive load test circuit

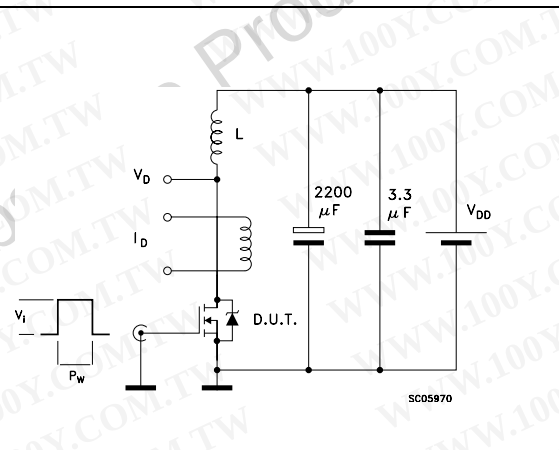


Figure 17. Unclamped inductive waveform

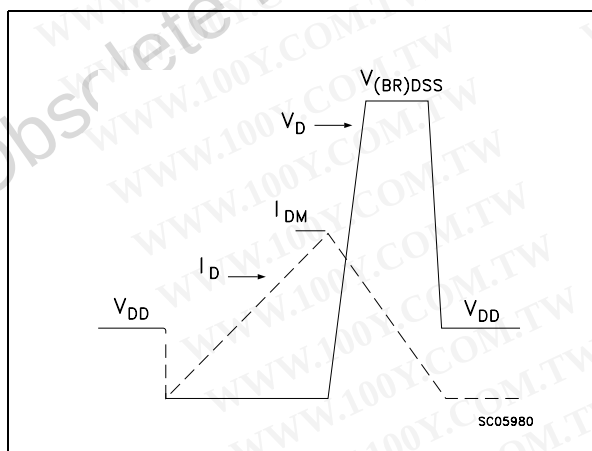
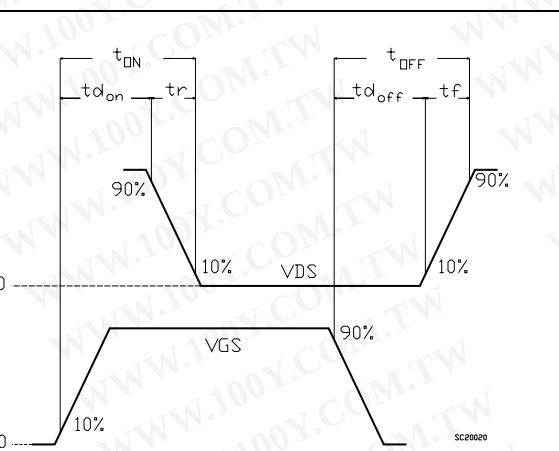
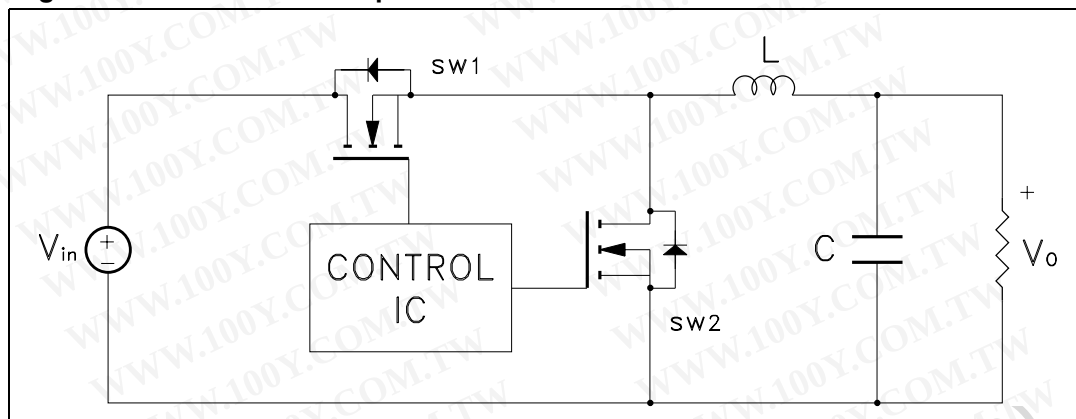


Figure 18. Switching time waveform



4 Appendix A

Figure 19. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
 - Very low $R_{DS(on)}$ to reduce conduction losses
 - Small Q_{gl} s to reduce the gate charge losses
 - Small C_{oss} to reduce losses due to output capacitance
 - Small Q_{rr} to reduce losses on SW1 during its turn-on
 - The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
 - Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
 - Small Q_g to have a faster commutation and to reduce gate charge losses
 - Low $R_{DS(on)}$ to reduce the conduction losses.

Table 6. Power losses calculation

		High side switching (SW1)	Low side switch (SW2)
Pconduction		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
Pswitching		$V_{in} * (Q_{gth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
Pdiode	Recovery (1)	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(Q _G)		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P _{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

Table 7. Paramiters meaning

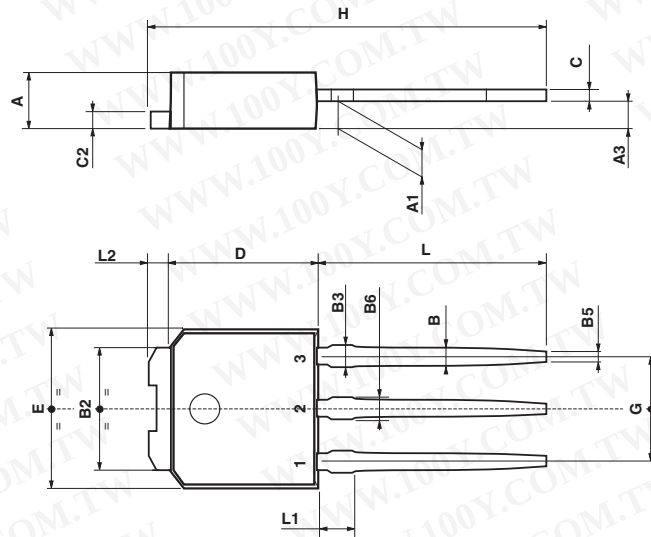
Parameter	Meaning
d	Duty-cycle
Q _{gth}	Post threshold gate charge
Q _{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P _{Qoss}	Output capacitance losses

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-251 (IPAK) MECHANICAL DATA

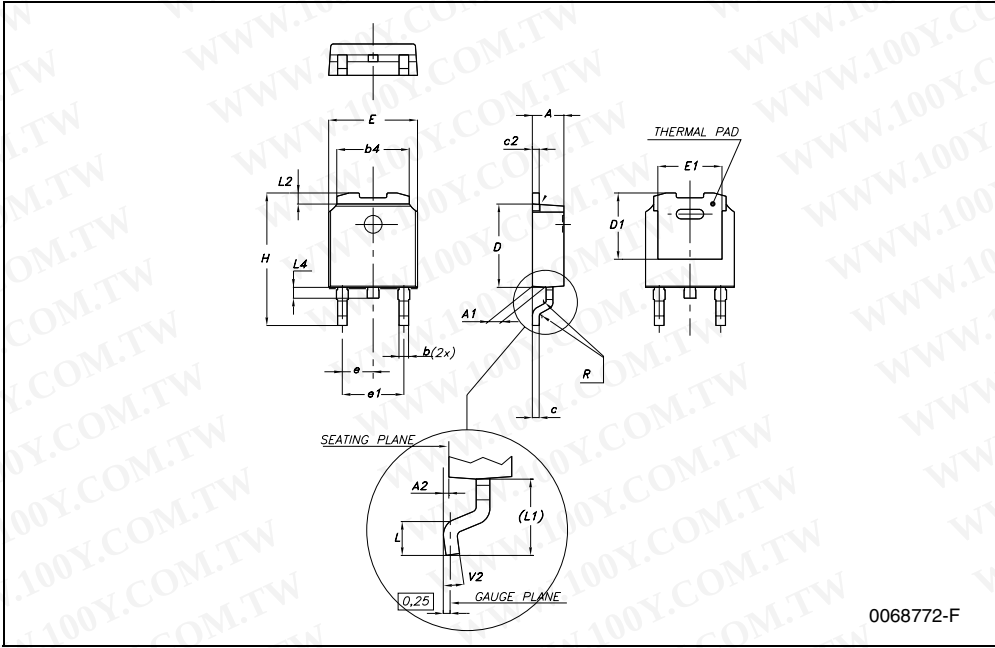
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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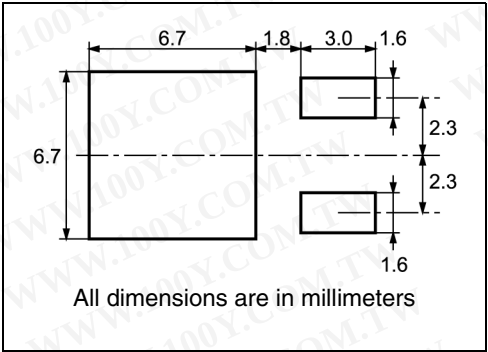
DPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

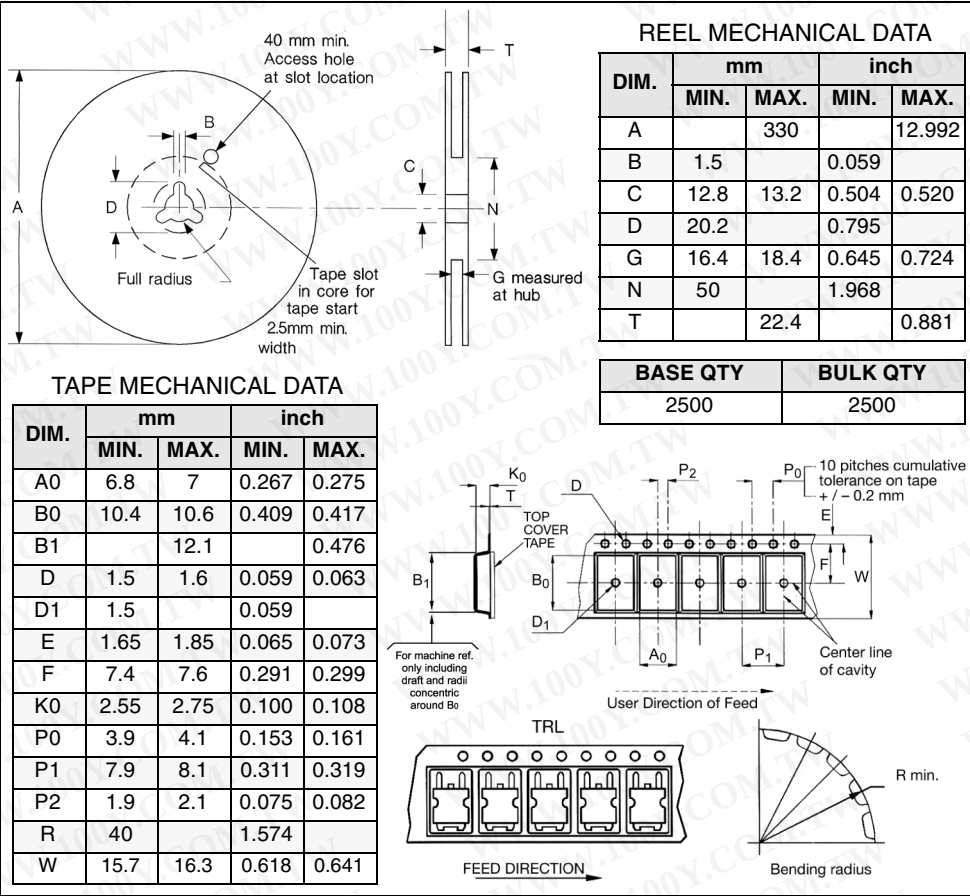


6 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



7 Revision history

Table 8. Revision history

Date	Revision	Changes
22-Jun-2004	2	Preliminary datasheet
21-Jul-2005	3	Complete version
13-Jun-2006	4	Packing mechanical data inserted
16-Jul-2006	5	New template, no content change

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