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STD12NF06 STD12NF06T4

N-channel 60 V, 0.08 Ω , 12 A, DPAK, IPAK
 STripFET™ II Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STD12NF06	60V	<0.1 Ω	12A
STD12NF06T4	60V	<0.1 Ω	12A

- Exceptional dv/dt capability
- Low gate charge

Applications

- Switching application

Description

This Power MOSFET is the latest development of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

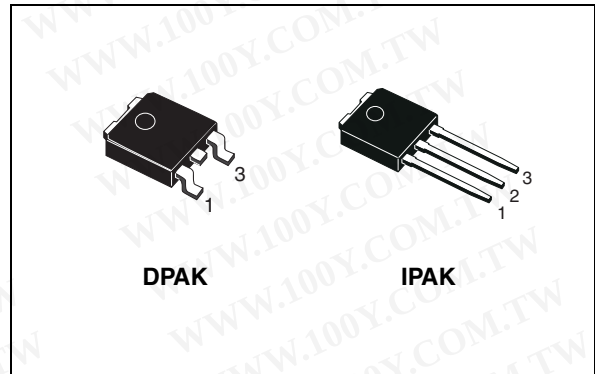


Figure 1. Internal schematic diagram

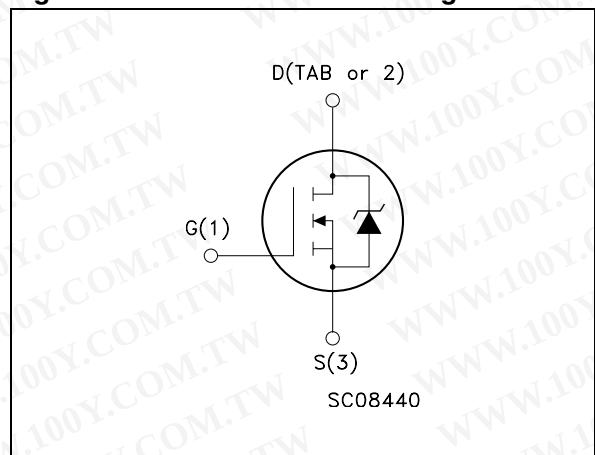


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD12NF06T4T4	D12NF06	DPAK	Tape and reel
STD12NF06T4-1	D12NF06	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ C$	12	A
I_D	Drain current (continuous) at $T_C = 100^\circ C$	8.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at $T_C = 25^\circ C$	30	W
	Derating factor	0.2	W/ $^\circ C$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	140	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ C$
T_J	Max. operating junction temperature		

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 12$ A, $di/dt \leq 200$ A/ μs , $V_{DS} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

3. Starting $T_J = 25^\circ C$, $I_D = 6$ A, $V_{DD} = 30$ V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case Max	5	$^\circ C/W$
R_{thJA}	Thermal resistance junction-ambient Max	100	$^\circ C/W$
T_I	Maximum lead temperature for soldering purpose	275	$^\circ C$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 25\text{mA}$, $V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 6\text{A}$		0.08	0.1	W

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 6\text{A}$	-	5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$	-	315 70 30		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 48\text{V}$, $I_D = 12\text{A}$ $V_{GS} = 10\text{V}$	-	10 3.0 3.5	12	nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{V}$, $I_D = 6\text{A}$,		7		ns
t_r	Rise time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$		18		ns
$t_{d(off)}$	Turn-off delay time		-	17	-	ns
t_f	Fall time	Figure 14 on page 8		6		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM}	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 12A$, $V_{GS} = 0$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 12A$, $di/dt = 100A/\mu s$, $V_{DD} = 30V$, $T_J = 150^\circ C$ <i>Figure 16 on page 8</i>	-	50		ns
Q_{rr}	Reverse recovery charge			65		nC
I_{RRM}	Reverse recovery current			3.5		A

1. Pulsed: pulse duration= 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

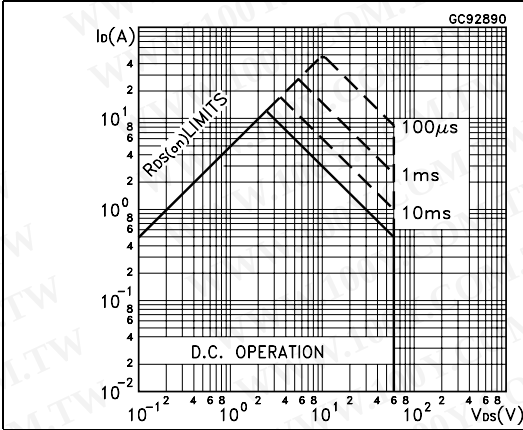


Figure 3. Thermal impedance

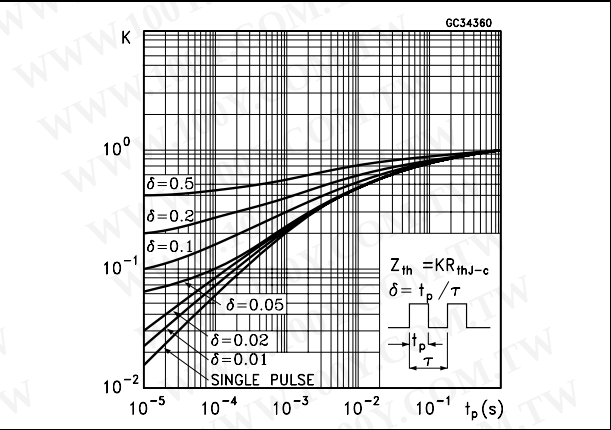


Figure 4. Output characteristics

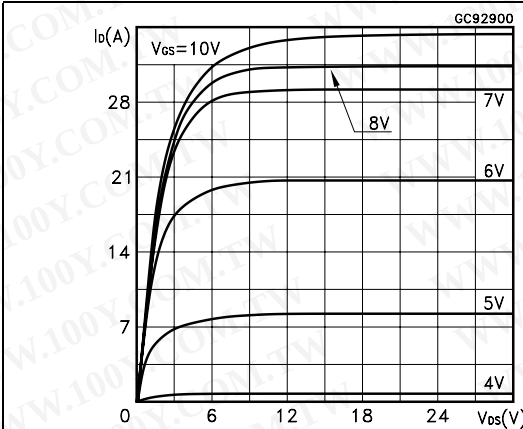


Figure 5. Transfer characteristics

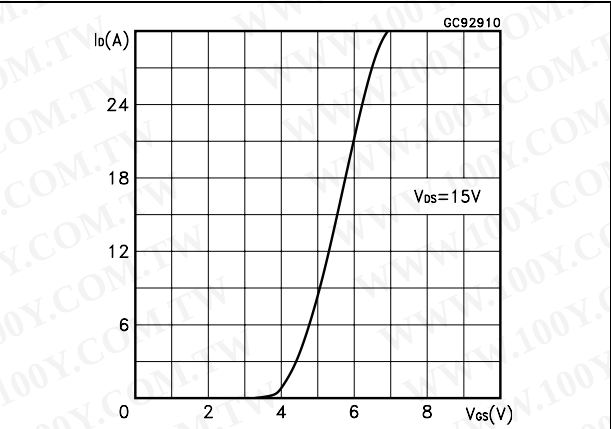


Figure 6. Transconductance

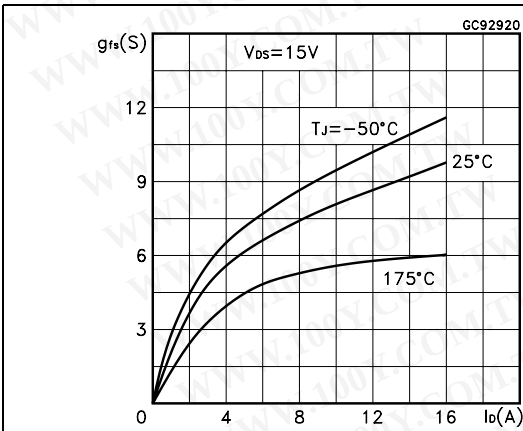


Figure 7. Static drain-source on resistance

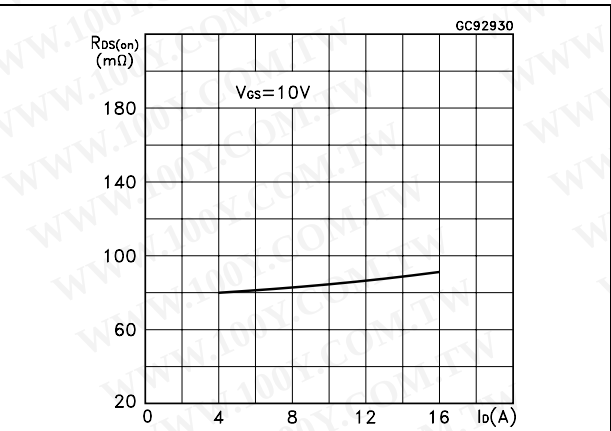
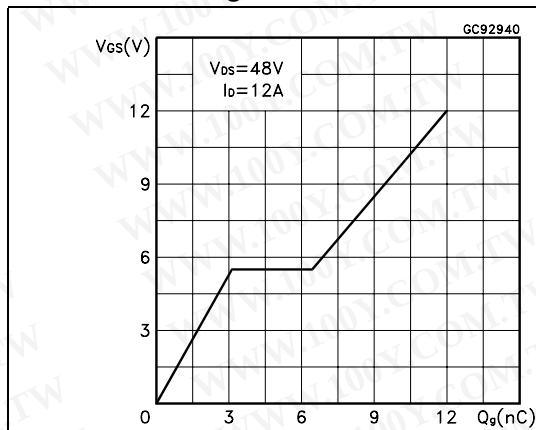
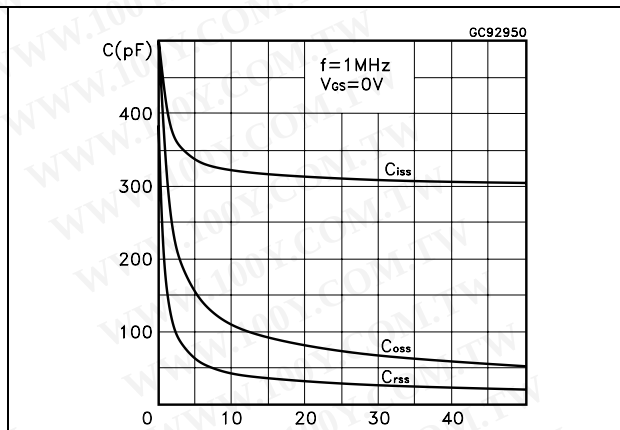
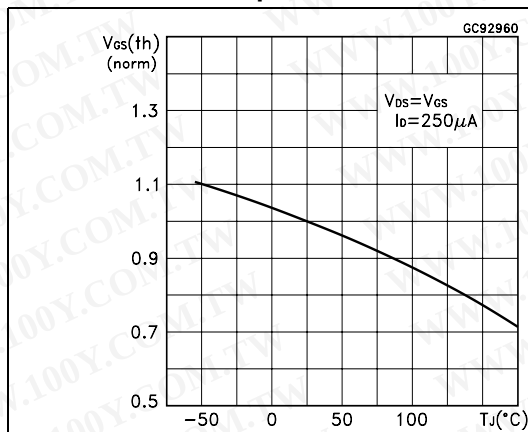
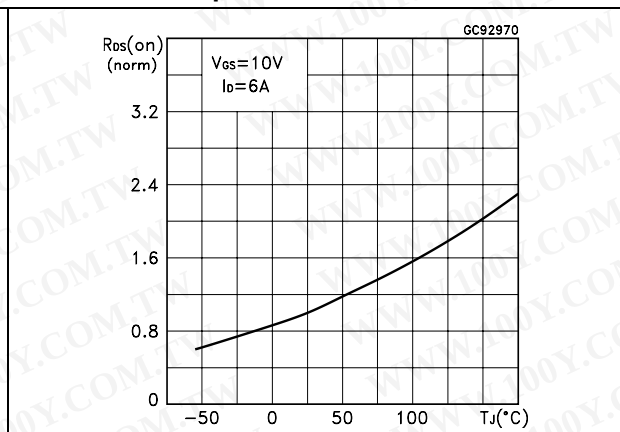
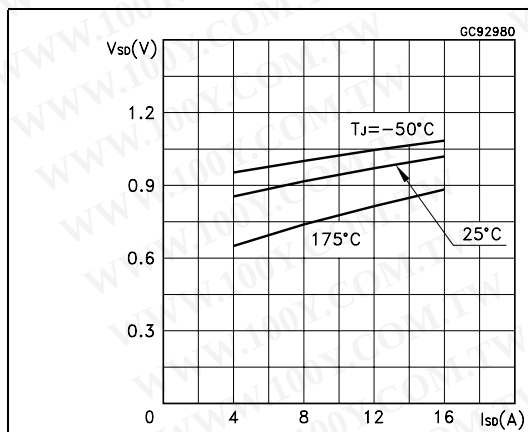
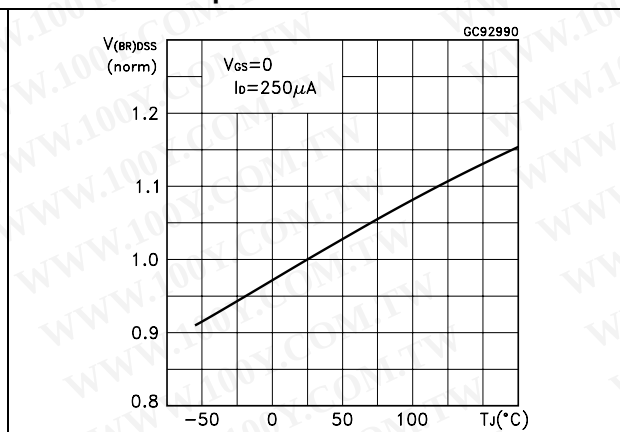


Figure 8. Gate charge vs. gate-source voltage**Figure 9. Capacitance variations****Figure 10. Normalized gate threshold voltage vs. temperature****Figure 11. Normalized on resistance vs. temperature****Figure 12. Source-drain diode forward characteristics****Figure 13. Normalized breakdown voltage vs. temperature**

3 Test circuits

Figure 14. Switching times test circuit for resistive load

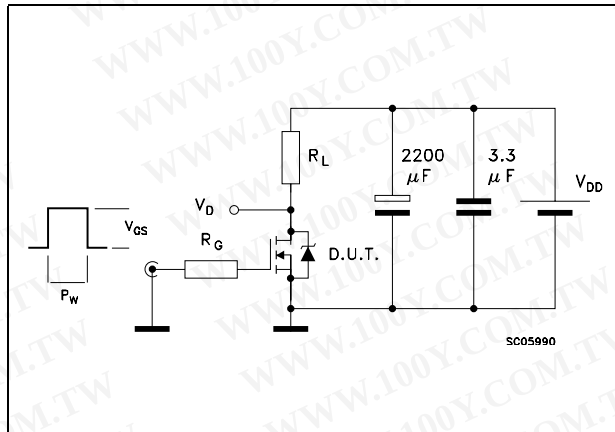


Figure 15. Gate charge test circuit

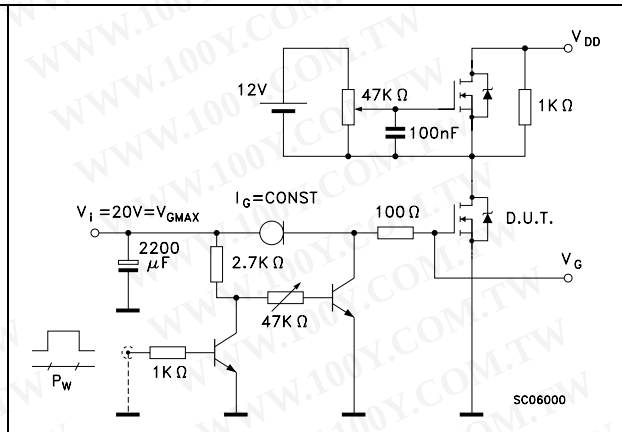


Figure 16. Test circuit for inductive load switching and diode recovery times

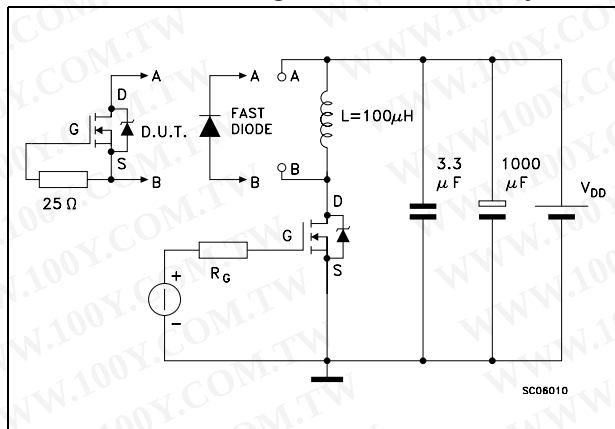


Figure 17. Unclamped inductive load test circuit

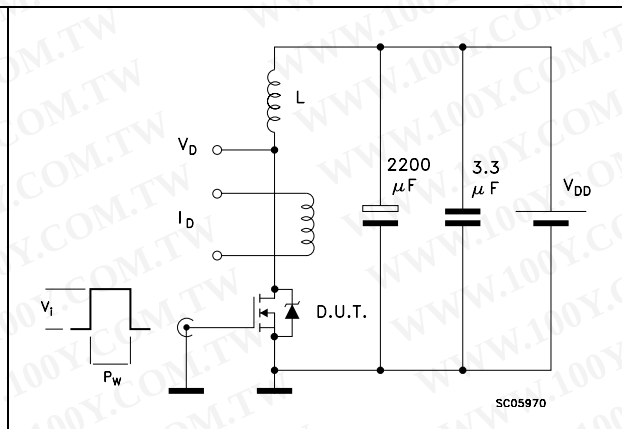
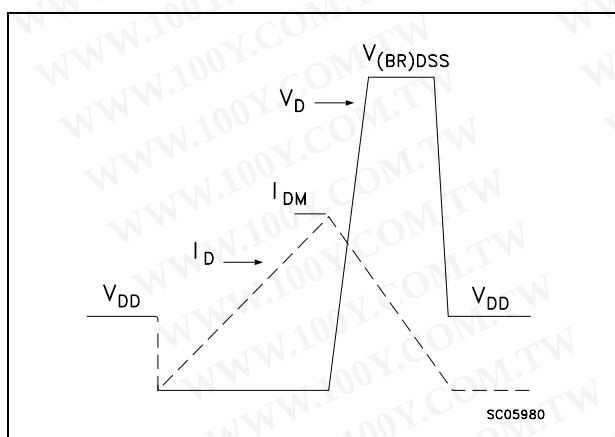


Figure 18. Unclamped inductive waveform

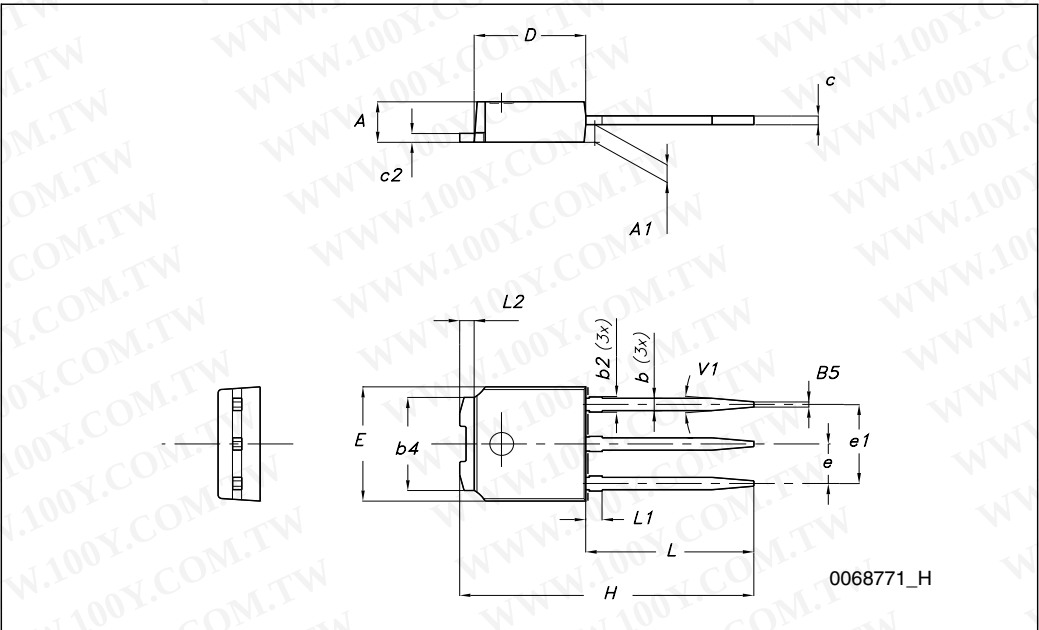


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

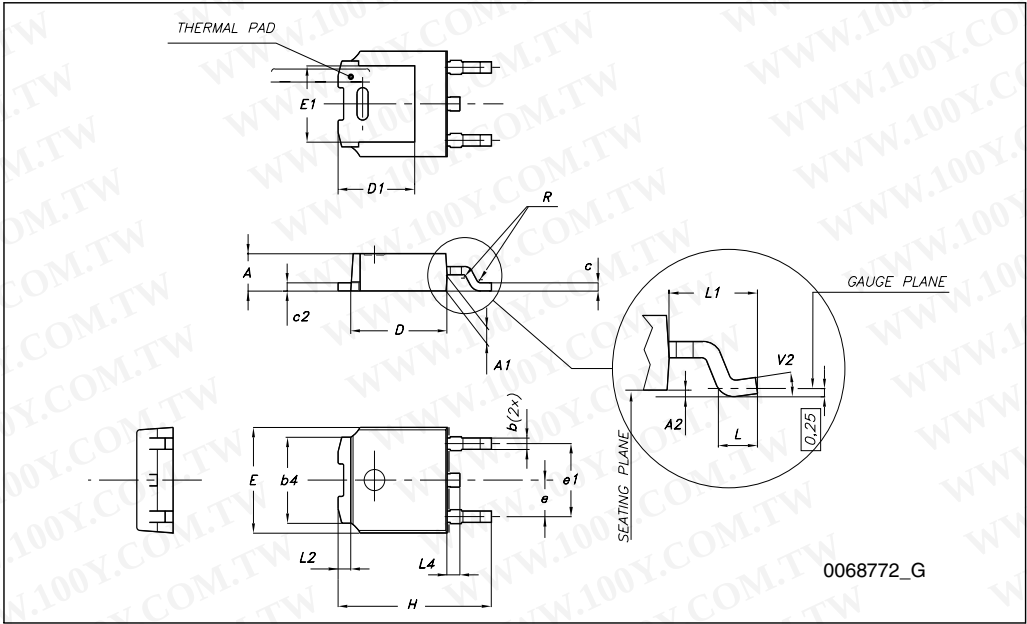
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10 °	



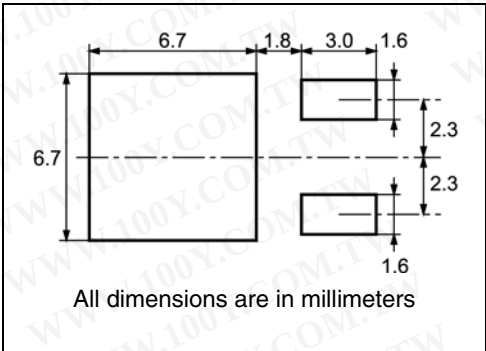
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

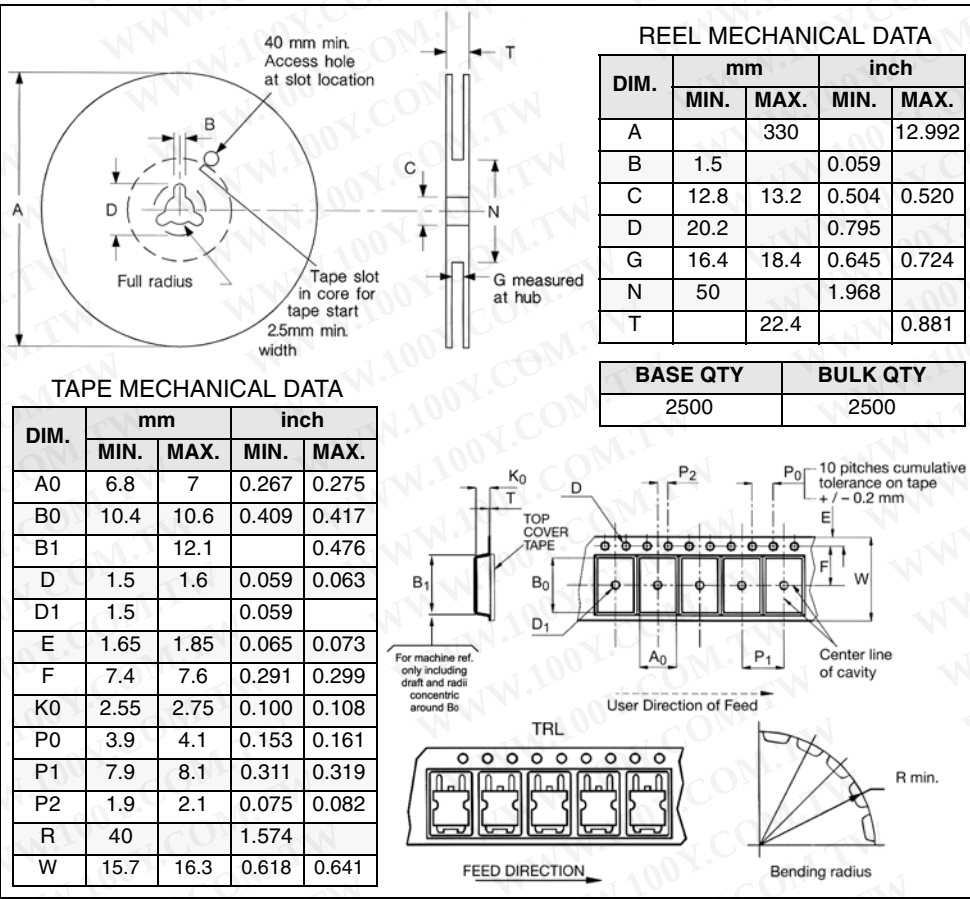


5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
09-Sep-2004	3	Complete document
07-Aug-2006	4	The document has been reformatted
19-Feb-2007	5	Typo mistake on page 1
15-Apr-2009	6	Table 1: Device summary has been updated Mechanical data updated
26-Nov-2009	7	Updated Q_{rr} in Table 7: Source drain diode .

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