



Dual N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
60	0.060 at V _{GS} = 10 V	4.8	13
	0.075 at V _{GS} = 4.5 V	4.3	

FEATURES

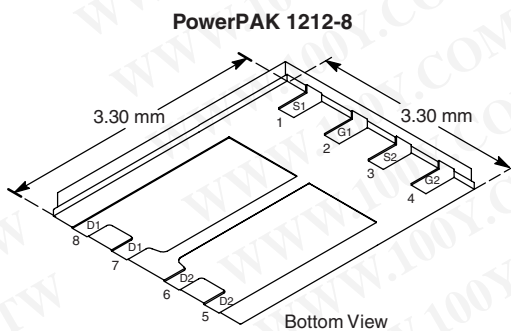
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package, 1/3 the Space of An SO-8 While Thermally Comparable



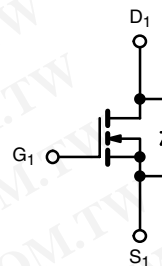
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

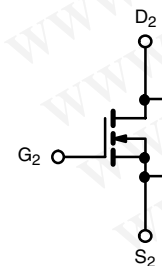
- Synchronous Rectification
- Primary Side Switch



Ordering Information: Si7220DN-T1-E3 (Lead (Pb)-free)
Si7220DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	V _{DS}	60		V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	4.8	3.4	A
		T _A = 70 °C	3.8	2.7	
Pulsed Drain Current	I _{DM}	20		mJ	
Avalanche Current	I _{AS}	11			
Single Avalanche Energy	E _{AS}	6.1			
Continuous Source Current (Diode Conduction) ^a	I _S	2.2	1.1	A	
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	2.6	1.3	W
		T _A = 70 °C	1.4	0.69	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	38	48	°C/W
		Steady State	77	94	
Maximum Junction-to-Case (Drain)	R _{thJC}	4.3	5.4		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

Si7220DN

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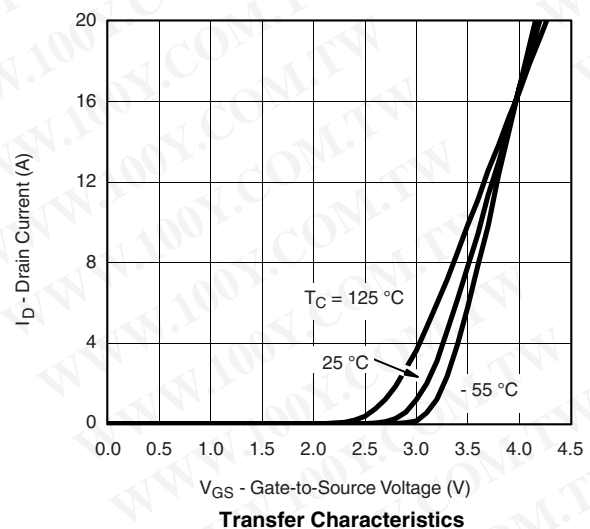
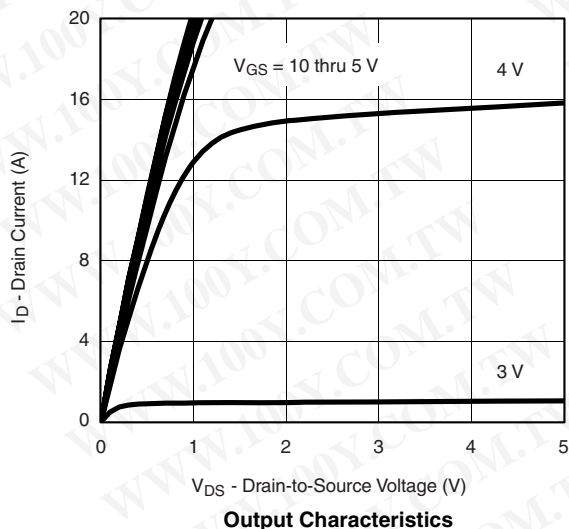
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1		3	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 4.8 \text{ A}$		0.048	0.060	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 4.3 \text{ A}$		0.061	0.075	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 4.8 \text{ A}$		15		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.2 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4.8 \text{ A}$		13	20	nC
Gate-Source Charge	Q_{gs}		2.3			
Gate-Drain Charge	Q_{gd}		2.6			
Gate Resistance	R_g	$f = 1 \text{ MHz}$		2		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30 \text{ V}, R_L = 30 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$		10	15	ns
Rise Time	t_r		10			
Turn-Off Delay Time	$t_{d(off)}$		20			
Fall Time	t_f		10			
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		30	60	

Notes:

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

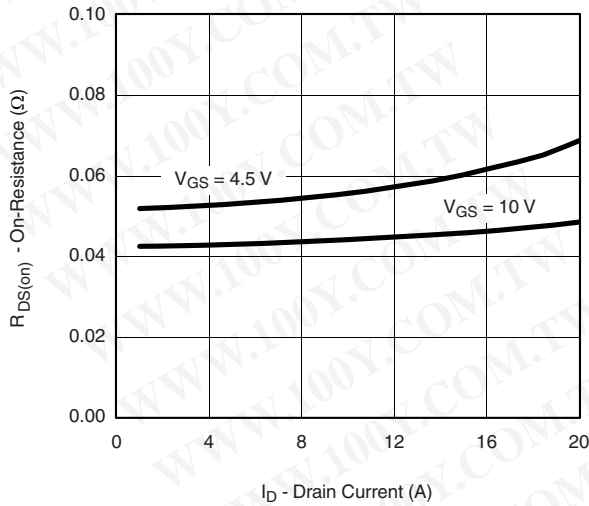




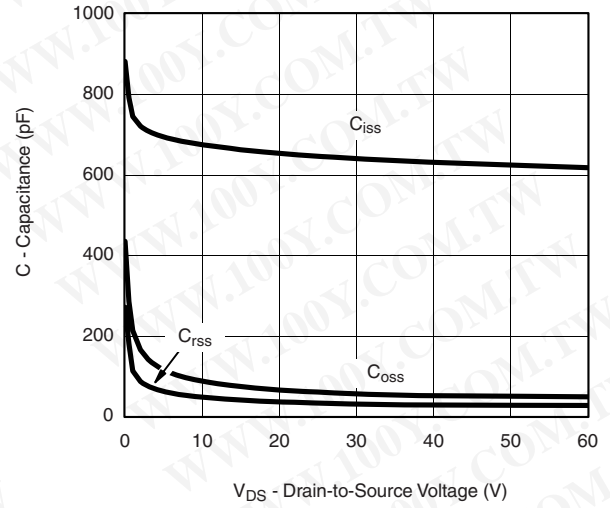
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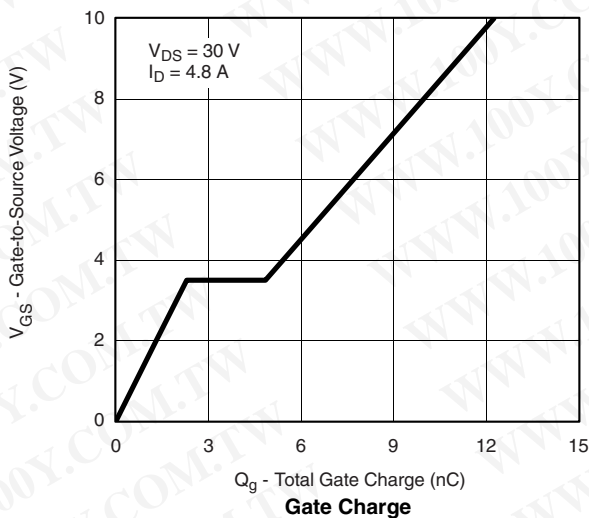
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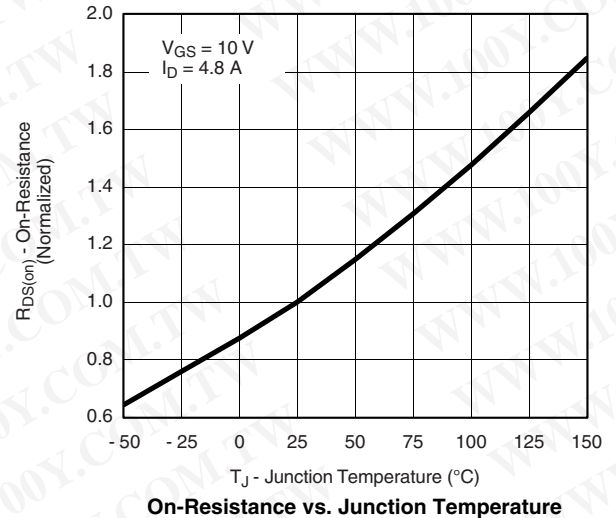
On-Resistance vs. Drain Current



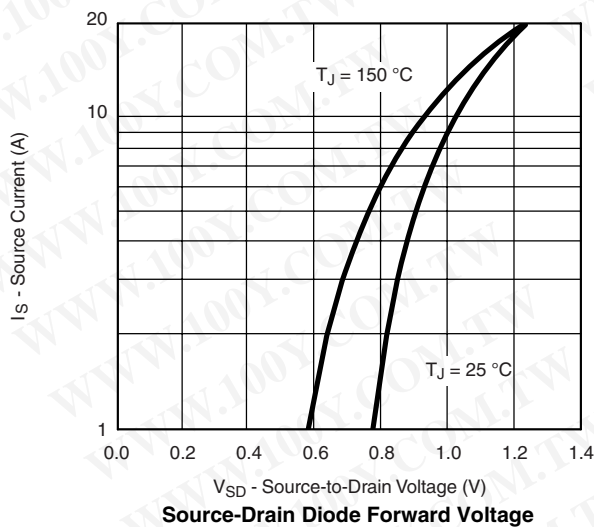
Capacitance



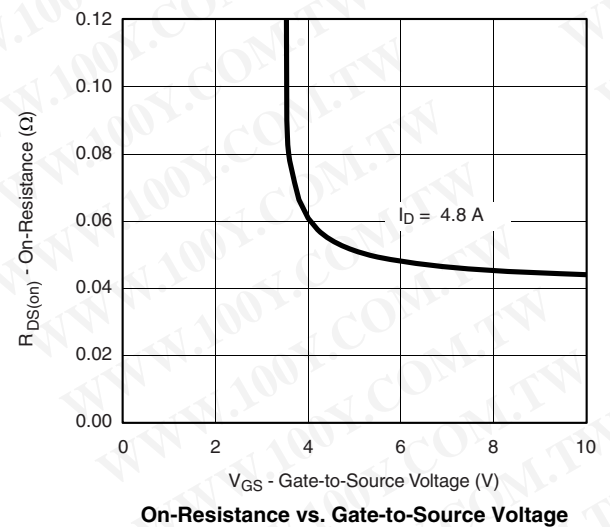
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

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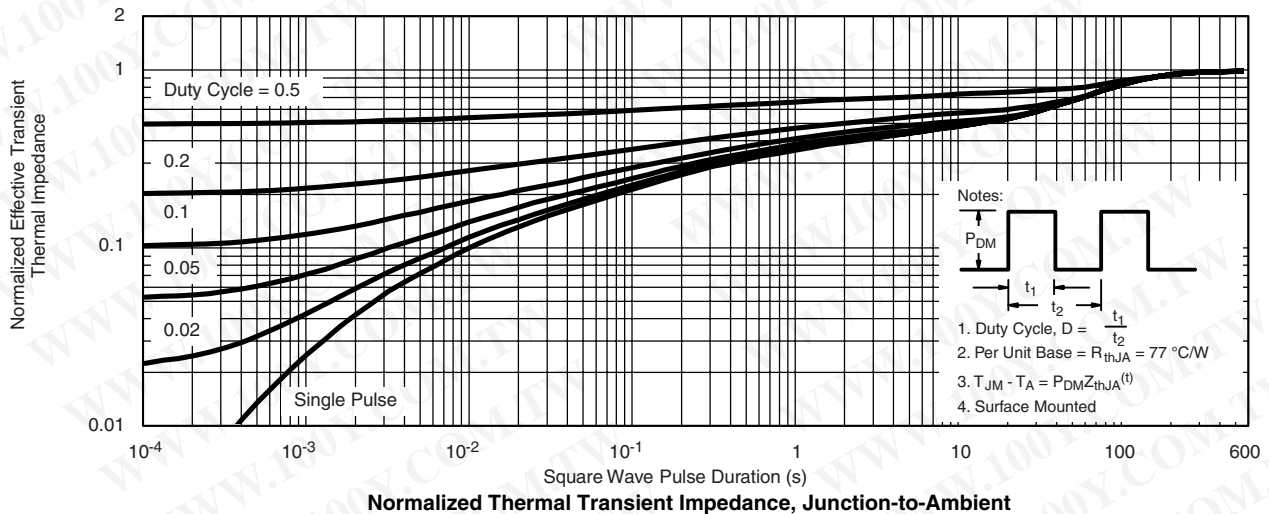
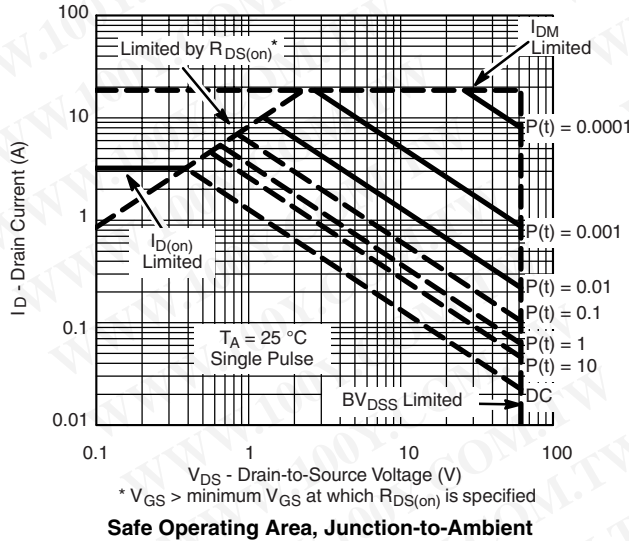
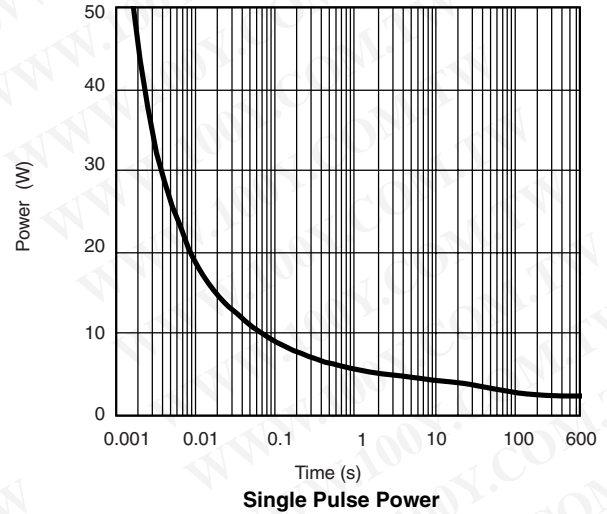
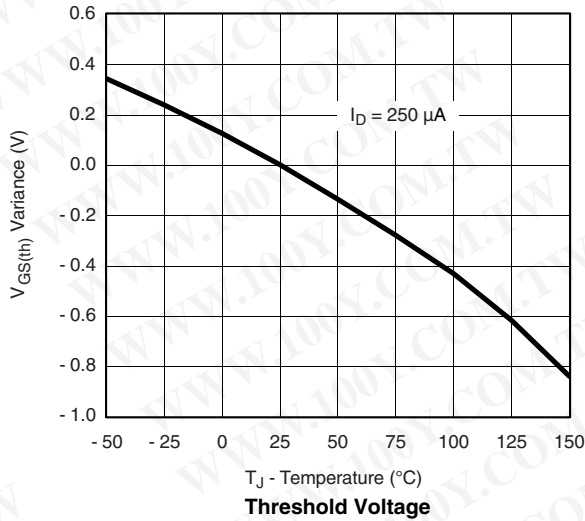
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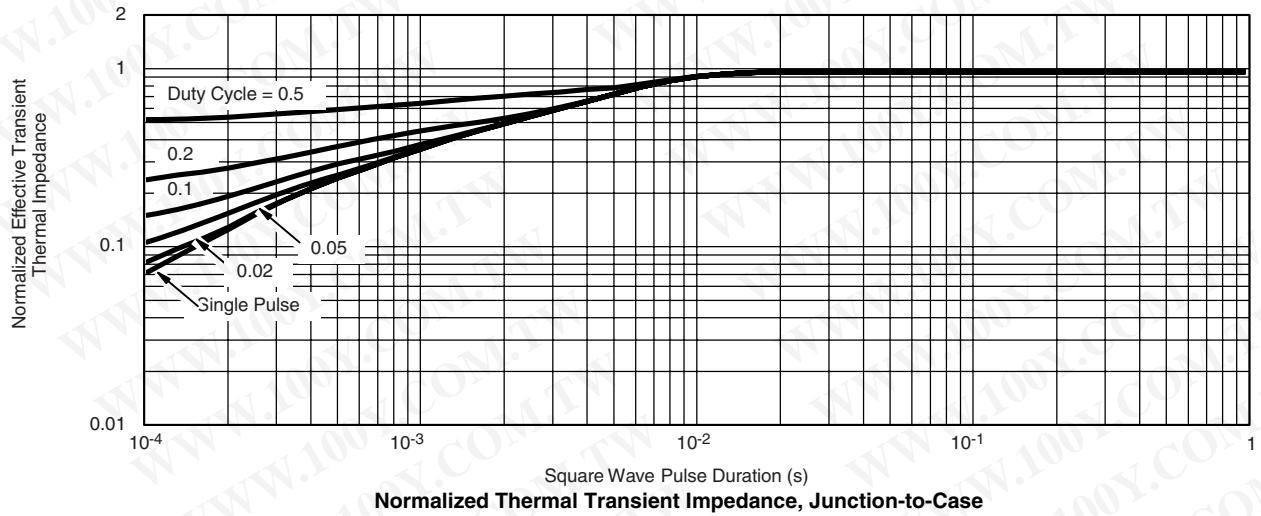


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Notes:
The minimum creepage between D1 and D2 for this 100 V device is 0.2 mm. Please see PowerPAK 1212-8 outline drawing, document # 71656, for more information.

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