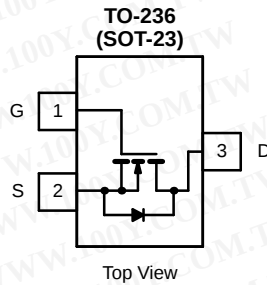




N-Channel 1.25-W, 2.5-V MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.085 @ $V_{GS} = 4.5$ V	2.8
	0.115 @ $V_{GS} = 2.5$ V	2.4



Si2302DS (A2)*

*Marking Code

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ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^b	I_D	2.8	A
		2.2	
Pulsed Drain Current ^a	I_{DM}	10	
Continuous Source Current (Diode Conduction) ^b	I_S	1.6	
Power Dissipation ^b	P_D	1.25	W
		0.80	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^b	R_{thJA}	100	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^c		166	

Notes

- Pulse width limited by maximum junction temperature.
- Surface Mounted on FR4 Board, $t \leq 5$ sec.
- Surface Mounted on FR4 Board.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

**SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 10\text{ }\mu\text{A}$	20			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	0.65			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	6			A
		$V_{DS} \geq 5\text{ V}, V_{GS} = 2.5\text{ V}$	4			
Drain-Source On-Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 3.6\text{ A}$		0.07	0.085	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 3.1\text{ A}$		0.085	0.115	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 5\text{ V}, I_D = 3.6\text{ A}$		10		S
Diode Forward Voltage	V_{SD}	$I_S = 1.6\text{ A}, V_{GS} = 0\text{ V}$		0.76	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 3.6\text{ A}$		5.4	10	nC
Gate-Source Charge	Q_{gs}			0.65		
Gate-Drain Charge	Q_{gd}			1.60		
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		340		pF
Output Capacitance	C_{oss}			115		
Reverse Transfer Capacitance	C_{rss}			33		
Switching						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 5.5\text{ }\Omega$ $I_D \cong 3.6\text{ A}, V_{GEN} = 4.5\text{ V}, R_G = 6\text{ }\Omega$		12	25	ns
Rise Time	t_r			36	60	
Turn-Off Delay Time	$t_{d(off)}$			34	60	
Fall-Time	t_f			10	25	

Notes

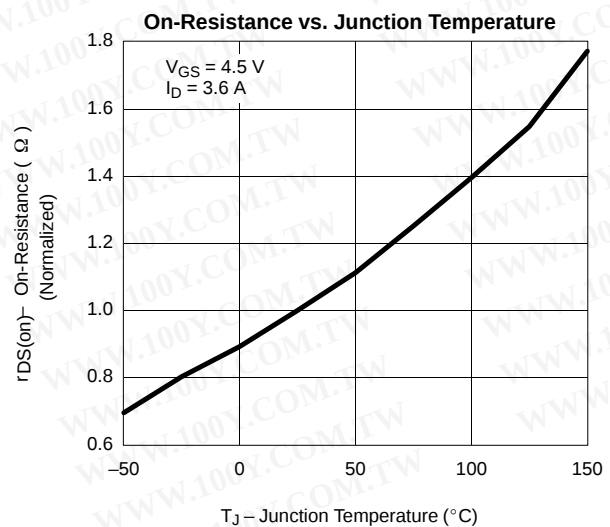
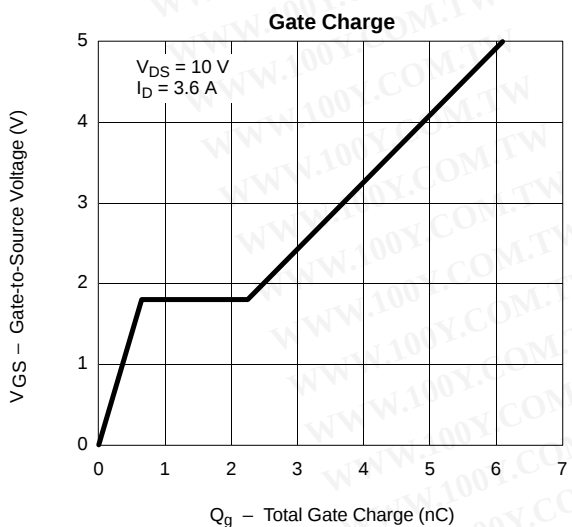
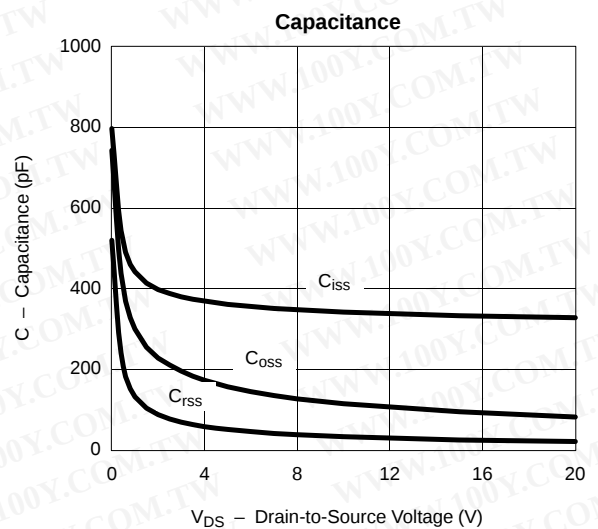
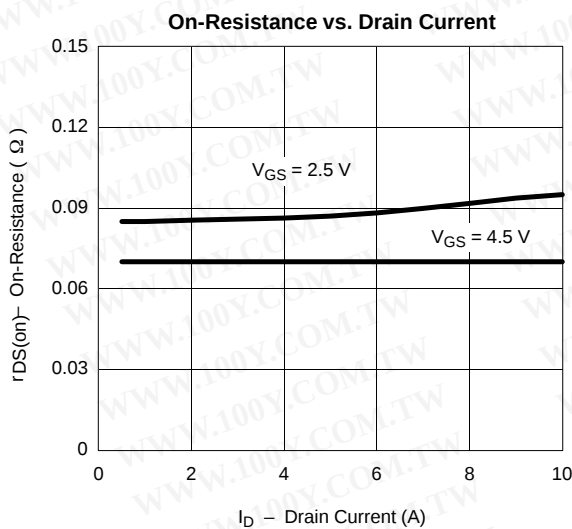
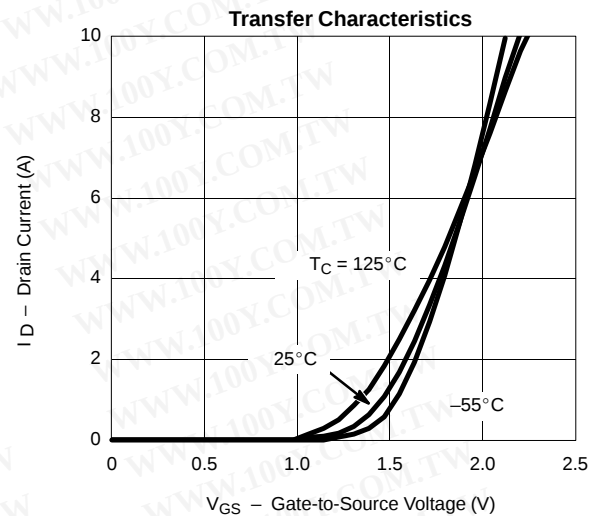
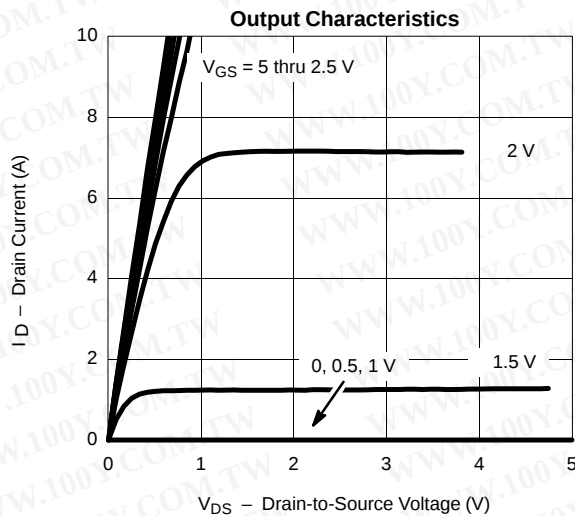
a. Pulse test: $PW \leq 300\text{ }\mu\text{s}$ duty cycle $\leq 2\%$.

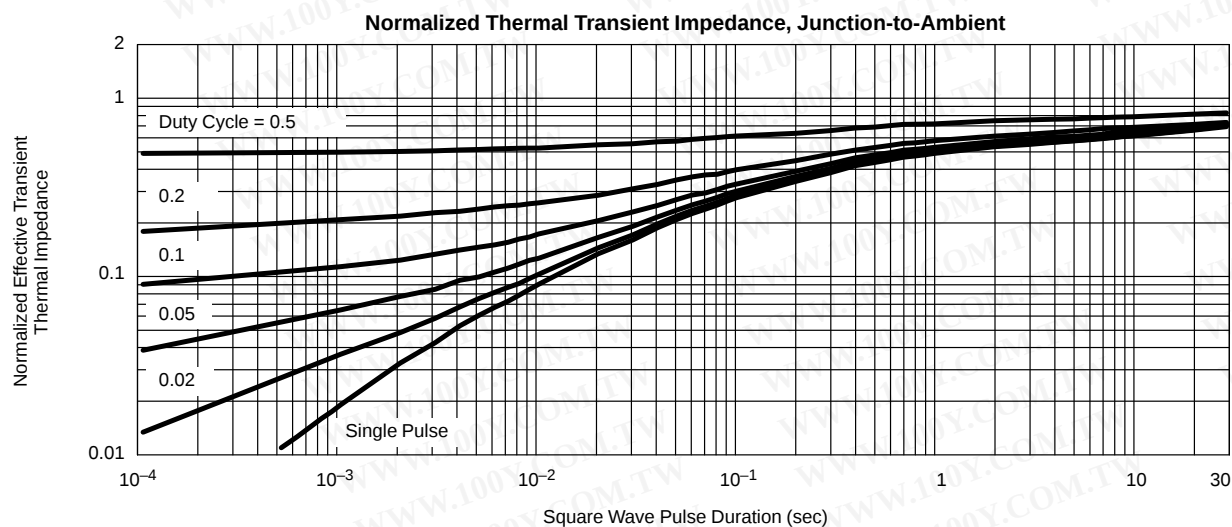
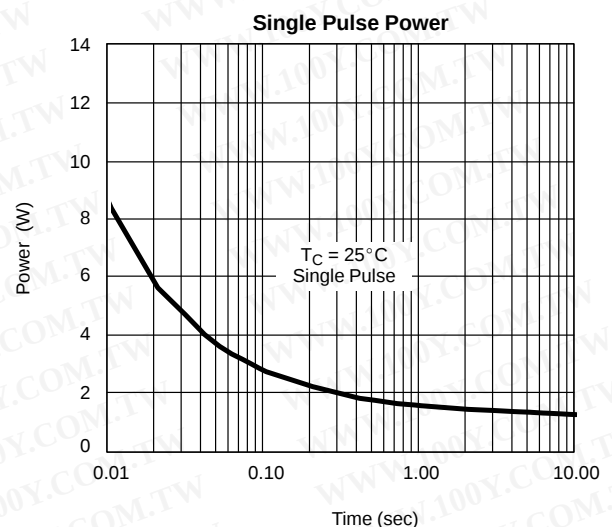
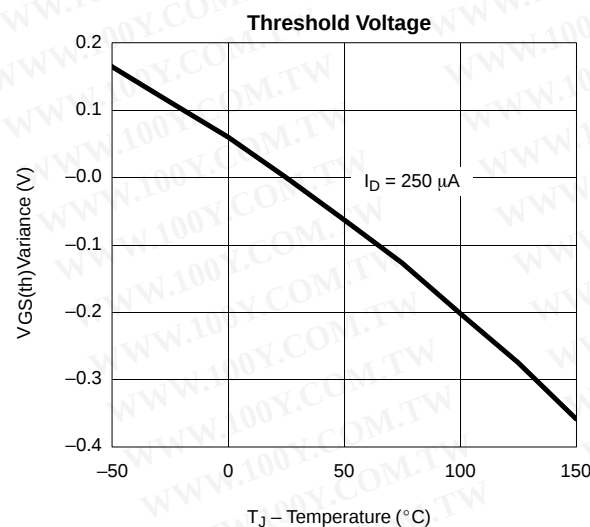
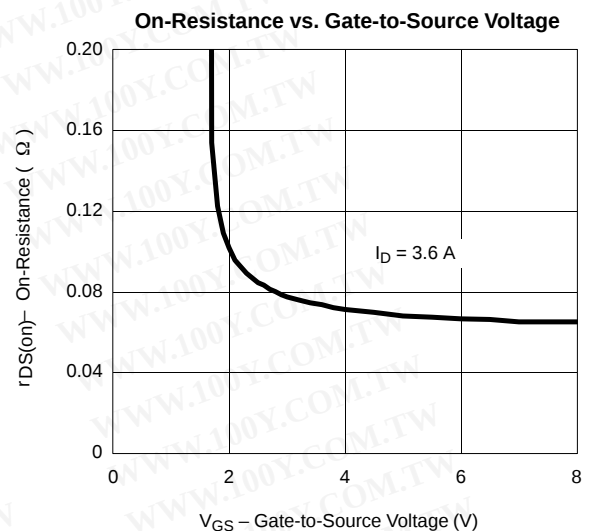
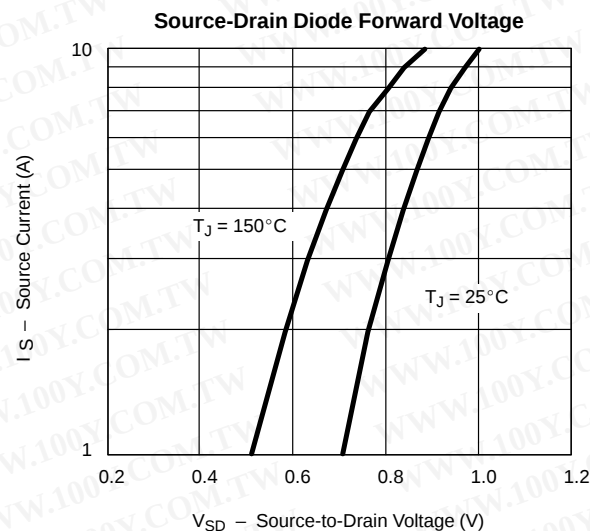
VNLR02

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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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