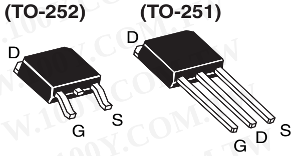
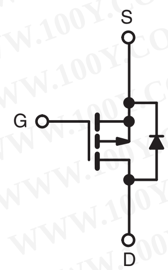
Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 50	
$R_{DS(on)}$ (Ω)	V_{GS} = - 10 V	0.50
Q_g (Max.) (nC)	9.1	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	5.9	
Configuration	Single	

DPAK (TO-252) IPAK (TO-251)





P-Channel MOSFET

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Surface Mountable (Order as IRFR9010, SiHFR9010)
- Straight Lead Option (Order as IRFU9010, SiHFU9010)
- Repetitive Avalanche Ratings
- Dynamic dV/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS* COMPLIANT
HALOGEN FREE Available

DESCRIPTION

The Power MOSFET technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt capability.

The Power MOSFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The DPAK (TO-252) surface mount package brings the advantages of Power MOSFETs to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9010, SiHFR9010 is provided on 16 mm tape. The straight lead option IRFU9010, SiHFU9010 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, dc-to-dc converters, and a wide range of consumer products.

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR9010-GE3	SiHFR9010TR-GE3[a]	SiHFR9010TRL-GE3[a]	SiHFU9010-GE3
Lead (Pb)-free	IRFR9010PbF	IRFR9010TRPbF[a]	IRFR9010TRLPbF[a]	IRFU9010PbF
	SiHFR9010-E3	SiHFR9010T-E3[a]	SiHFR9010TL-E3[a]	SiHFU9010-E3
SnPb	IRFR9010	IRFR9010TR[a]	IRFR9010TRL[a]	IRFU9010
	SiHFR9010	SiHFR9010T[a]	SiHFR9010TL[a]	SiHFU9010

Note
a. See device orientation.

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 50	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25 °C	I_D	- 5.3	A
		T_C = 100 °C		- 3.3	
Pulsed Drain Current[a]			I_{DM}	- 21	
Linear Derating Factor				0.20	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	136	mJ
Repetitive Avalanche Current[a]			I_{AR}	- 5.3	A
Repetitive Avalanche Energy[a]			E_{AR}	2.5	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	25	W
Peak Diode Recovery dV/dt[c]			dV/dt	5.8	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)[d]	for 10 s			300	

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
b. V_{DD} = - 25 V, starting T_J = 25 °C, L = 9.7 mH, R_g = 25 Ω, peak I_L = - 5.3 A.
c. $I_{SD} \leq$ - 5.3 A, dI/dt $\leq$ - 80 A/μs, $V_{DD} \leq$ 40 V, $T_J \leq$ 150 °C, suggested R_g = 24 Ω.
d. 0.063" (1.6 mm) from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

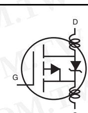
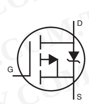
THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W
Case-to-Sink	R_{thCS}	-	1.7	-	
Maximum Junction-to-Case (Drain)[a]	R_{thJC}	-	-	5.0	

Note

a. Mounting pad must cover heatsink surface area.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA		- 50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = max. rating, V_{GS} = 0 V		-	-	- 250	µA
		V_{DS} = 0.8 x max. rating, V_{GS} = 0 V, T_J = 125 °C		-	-	- 1000	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = - 10 V	I_D = - 2.8 A[b]	-	0.35	0.5	Ω
Forward Transconductance	g_{fs}	V_{DS} ≤ - 50 V, I_{DS} = - 2.8 A		1.1	1.7	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1.0 MHz, see fig. 9		-	240	-	pF
Output Capacitance	C_{oss}			-	160	-	
Reverse Transfer Capacitance	C_{rss}			-	30	-	
Total Gate Charge	Q_g	V_{GS} = - 10 V	I_D = - 4.7 A, V_{DS} = 0.8 x max. rating, see fig. 16 (Independent operating temperature)	-	6.1	9.1	nC
Gate-Source Charge	Q_{gs}			-	2.0	3.0	
Gate-Drain Charge	Q_{gd}			-	3.9	5.9	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 25 V, I_D = - 4.7 A, R_g = 24 Ω, R_D = 5.6 Ω, see fig. 15 (Independent operating temperature)		-	6.1	9.2	ns
Rise Time	t_r			-	47	71	
Turn-Off Delay Time	$t_{d(off)}$			-	13	20	
Fall Time	t_f			-	35	59	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact. 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 5.3	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	- 18	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = - 5.3 A, V_{GS} = 0 V[b]		-	-	- 5.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = - 4,7 A, dI/dt = 100 A/µs[b]		33	75	160	ns
Body Diode Reverse Recovery Charge	Q_{rr}			0.090	0.22	0.52	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

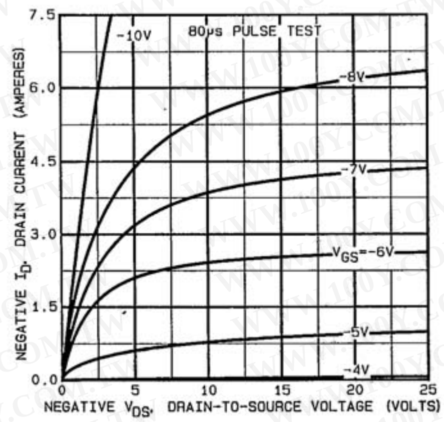


Fig. 1 - Typical Output Characteristics

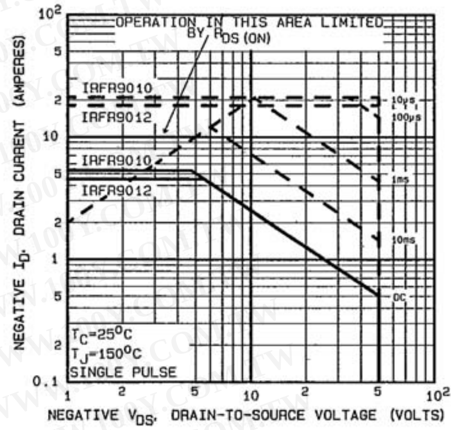


Fig. 4 - Maximum Safe Operating Area

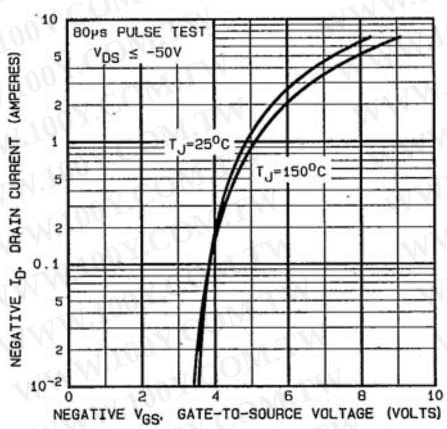


Fig. 2 - Typical Transfer Characteristics

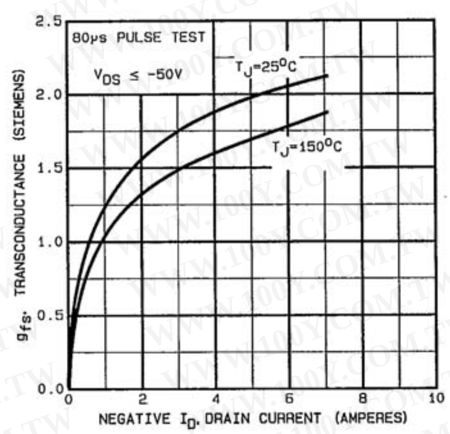


Fig. 5 - Typical Transconductance vs. Drain Current

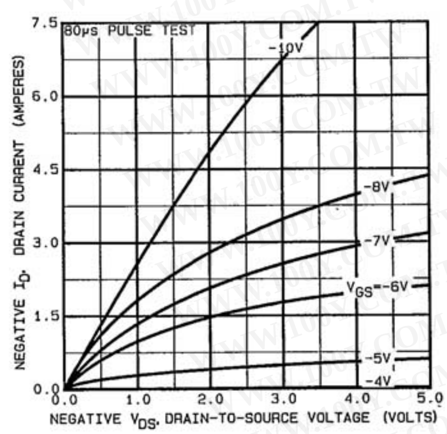


Fig. 3 - Typical Saturation Characteristics

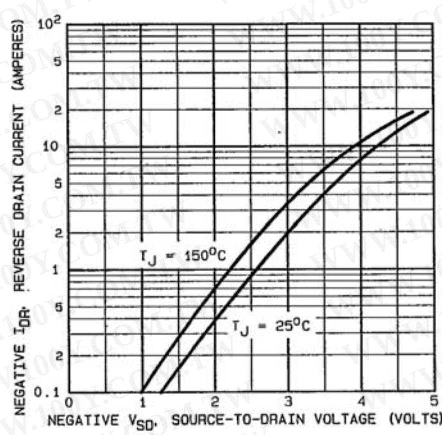


Fig. 6 - Typical Source-Drain Diode Forward Voltage

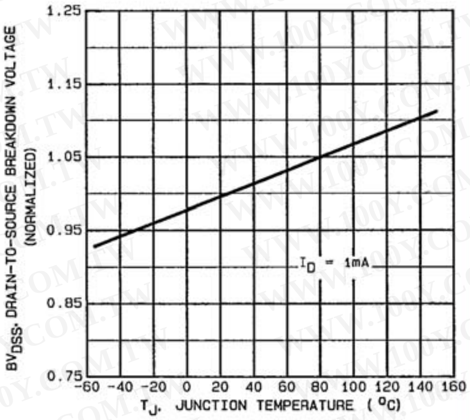


Fig. 7 - Breakdown Voltage vs. Temperature

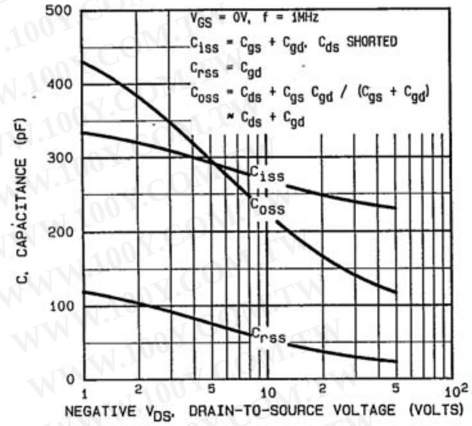


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

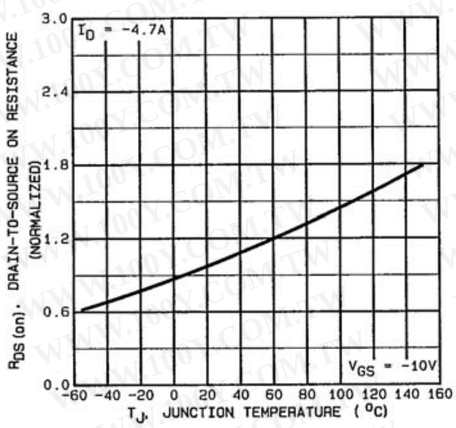


Fig. 8 - Normalized On-Resistance vs. Temperature

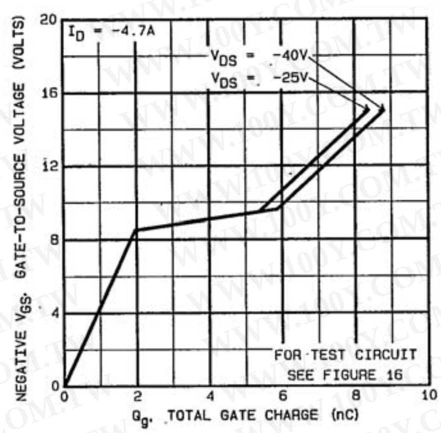


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

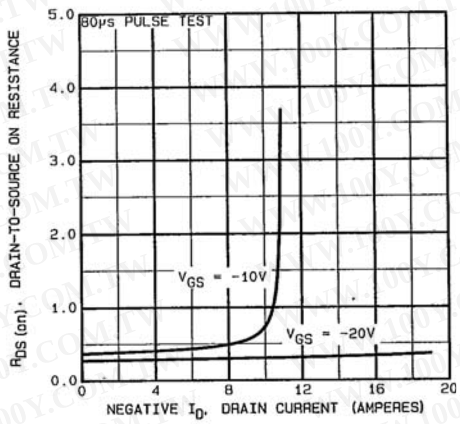


Fig. 11 - Typical On-Resistance vs. Drain Current

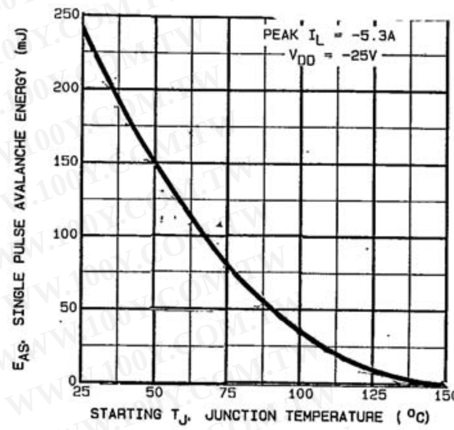


Fig. 13a - Maximum Avalanche vs. Starting Junction Temperature

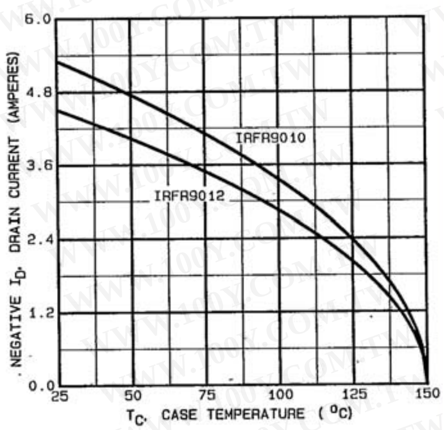


Fig. 12 - Maximum Drain Current vs. Case Temperature

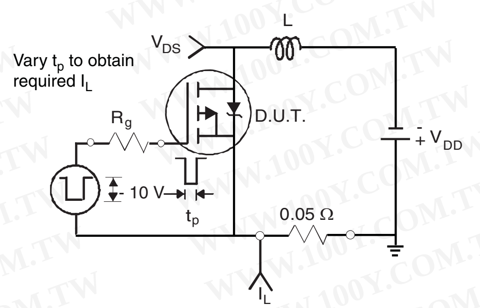


Fig. 13b - Unclamped Inductive Test Circuit

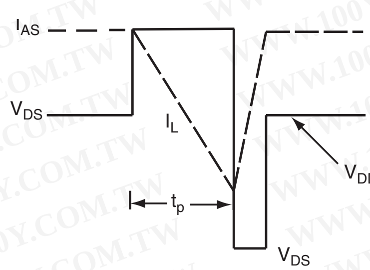


Fig. 13c - Unclamped Inductive Waveforms

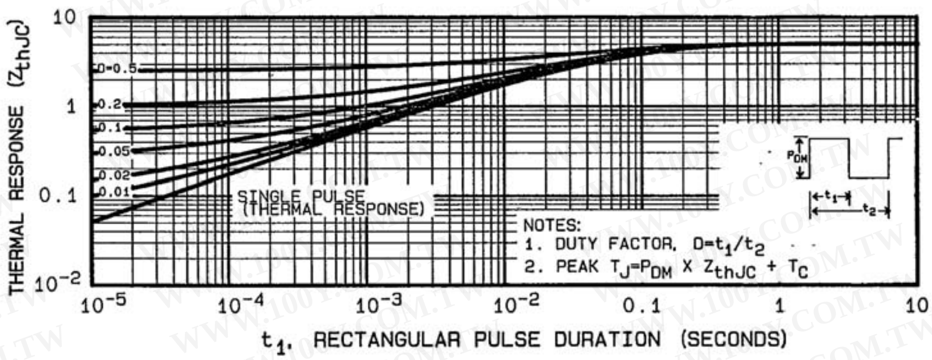


Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

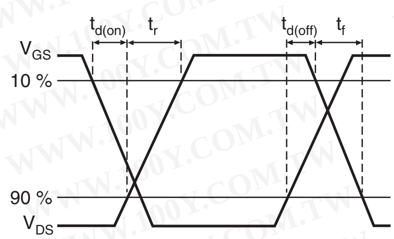


Fig. 15a - Switching Time Waveforms

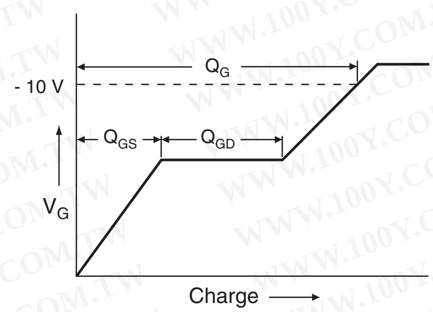


Fig. 16a - Basic Gate Charge Waveform

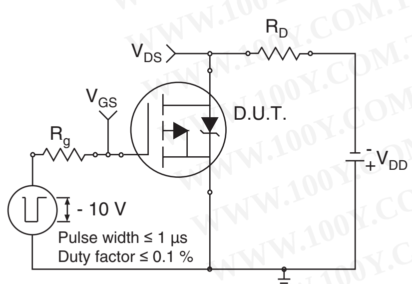


Fig. 15b - Switching Time Test Circuit

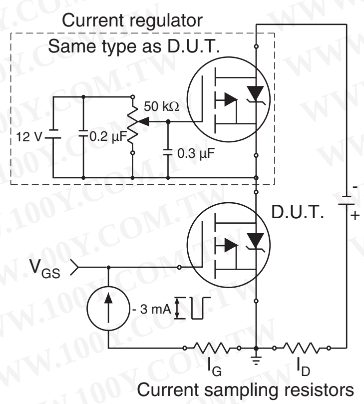
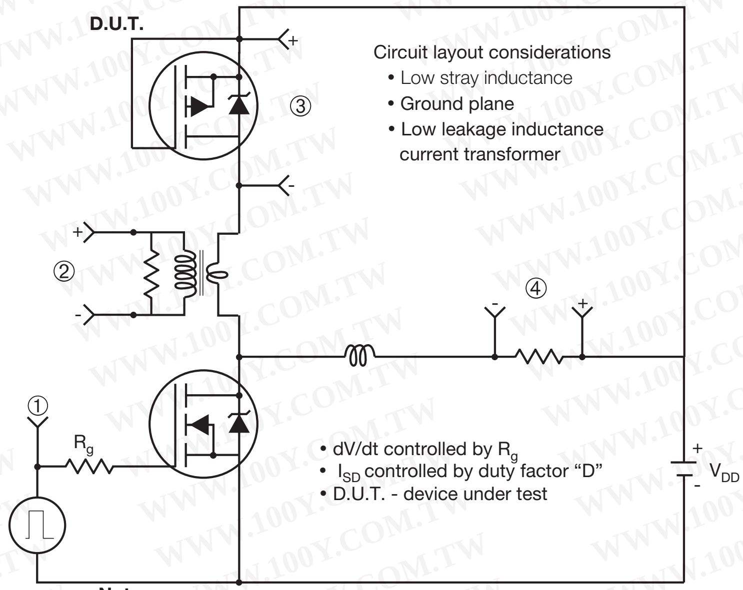
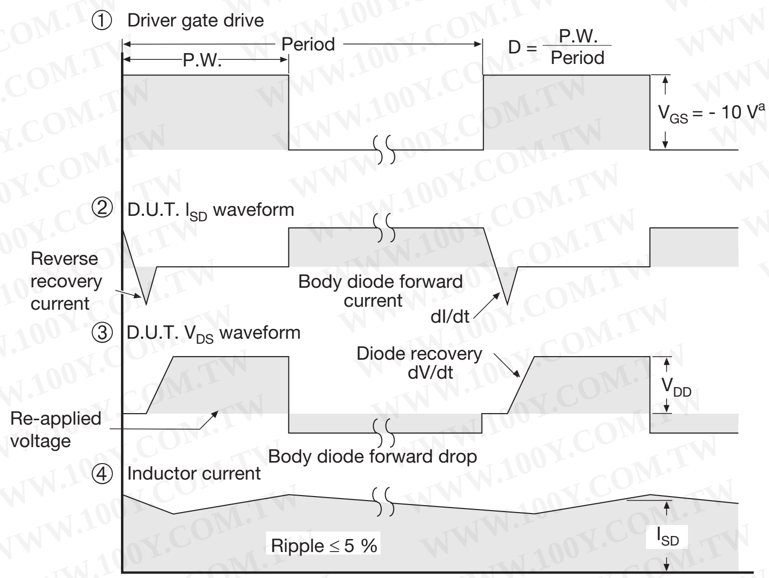


Fig. 16b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
- Compliment N-Channel of D.U.T. for driver



Note
a. V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 17 - For P-Channel

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