

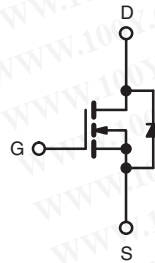
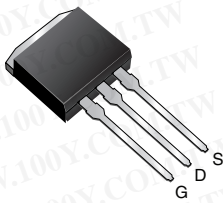


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Power MOSFET

| PRODUCT SUMMARY | | |
|---------------------------|-----------------|------|
| V_{DS} (V) | 500 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10$ V | 0.55 |
| Q_g (Max.) (nC) | 51 | |
| Q_{gs} (nC) | 12 | |
| Q_{gd} (nC) | 23 | |
| Configuration | Single | |

I²PAK (TO-262)



N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

| ORDERING INFORMATION | |
|----------------------|-----------------------------|
| Package | I ² PAK (TO-262) |
| Lead (Pb)-free | IRFSL11N50APbF |
| | SiHFSL11N50A-E3 |

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted) | | | | |
|---|----------------|--|---------------------|---|
| PARAMETER | SYMBOL | LIMIT | UNIT | |
| Drain-Source Voltage | V_{DS} | 500 | V | |
| Gate-Source Voltage | V_{GS} | ± 30 | | |
| Continuous Drain Current | I_D | V_{GS} at 10 V $T_C = 25^\circ\text{C}$ | 11 | A |
| | | $T_C = 100^\circ\text{C}$ | 7.0 | |
| Pulsed Drain Current ^a | I_{DM} | 44 | | |
| Linear Derating Factor | | 1.3 | W/ $^\circ\text{C}$ | |
| Single Pulse Avalanche Energy ^b | E_{AS} | 390 | mJ | |
| Repetitive Avalanche Current ^a | I_{AR} | 11 | A | |
| Repetitive Avalanche Energy ^a | E_{AR} | 19 | mJ | |
| Maximum Power Dissipation | P_D | 190 | W | |
| Peak Diode Recovery dV/dt ^c | dV/dt | 4.1 | V/ns | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to + 175 | $^\circ\text{C}$ | |
| Soldering Recommendations (Peak Temperature) | for 10 s | 300 ^d | | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25^\circ\text{C}$, $L = 6.4$ mH, $R_G = 25 \Omega$, $I_{AS} = 11$ A (see fig. 12).
- $I_{SD} \leq 11$ A, $di/dt \leq 185$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 175^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply



IRFSL11N50A, SiHFSL11N50A

Vishay Siliconix



| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.75 | |

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
|--|-----------------------|--|--|------|-----------|---------------|----|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$ | 500 | - | - | V | |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | - | 0.57 | - | V/°C | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 2.0 | - | 4.0 | V | |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 30\text{ V}$ | - | - | ± 100 | nA | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$ | - | - | 25 | μA | |
| | | $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$ | - | - | 250 | | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 6.6\text{ A}^b$ | - | - | 0.55 | Ω | |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}, I_D = 6.6\text{ A}^b$ | 6.0 | - | - | S | |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$, see fig. 5 | - | 1426 | - | pF | |
| Output Capacitance | C_{oss} | | - | 208 | - | | |
| Reverse Transfer Capacitance | C_{rss} | | - | 9.6 | - | | |
| Output Capacitance | C_{oss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$ | - | 1954 | - | |
| Effective Output Capacitance | $C_{oss\text{ eff.}}$ | | $V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$ | - | 53 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $V_{DS} = 0\text{ V to } 400\text{ V}^c$ | - | 110 | - | |
| Gate-Source Charge | Q_{GS} | | $I_D = 11\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 ^b | - | - | 51 | nC |
| Gate-Drain Charge | Q_{GD} | | | - | - | 23 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 250\text{ V}, I_D = 11\text{ A}$ $R_G = 9.1\text{ }\Omega, R_D = 22\text{ }\Omega$, see fig. 10 ^b | - | 14 | - | ns | |
| Rise Time | t_r | | - | 34 | - | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 32 | - | | |
| Fall Time | t_f | | - | 27 | - | | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact | - | 4.5 | - | nH | |
| Internal Source Inductance | L_S |  | - | 7.5 | - | | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode |  | - | - | 11 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | | - | - | 44 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 11\text{ A}, V_{GS} = 0\text{ V}^b$ | - | - | 1.5 | V | |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 11\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$ | - | 530 | 790 | ns | |
| Body Diode Reverse Recovery Charge | Q_{rr} | | - | 3.4 | 5.1 | μC | |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80% V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

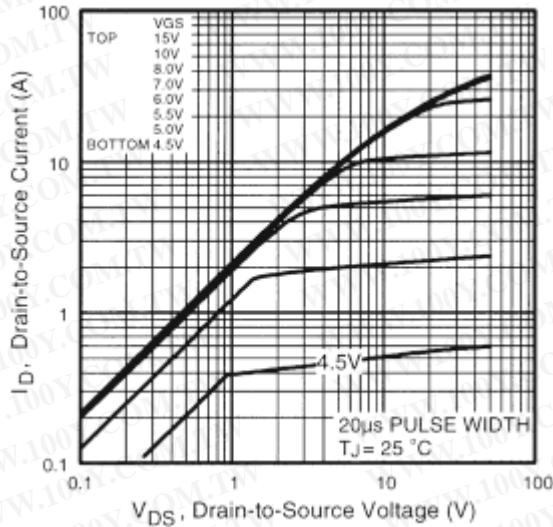


Fig. 1 - Typical Output Characteristics

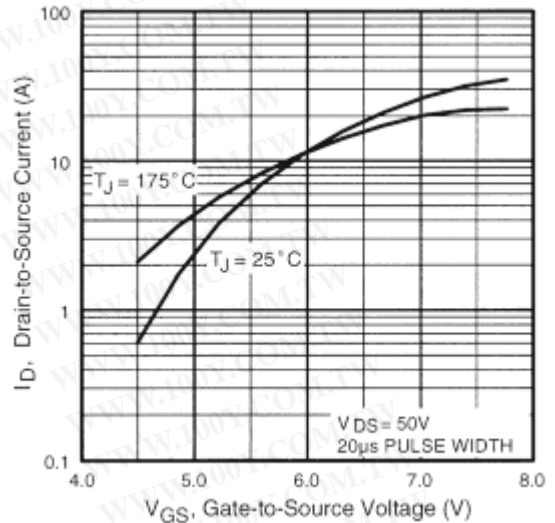


Fig. 3 - Typical Transfer Characteristics

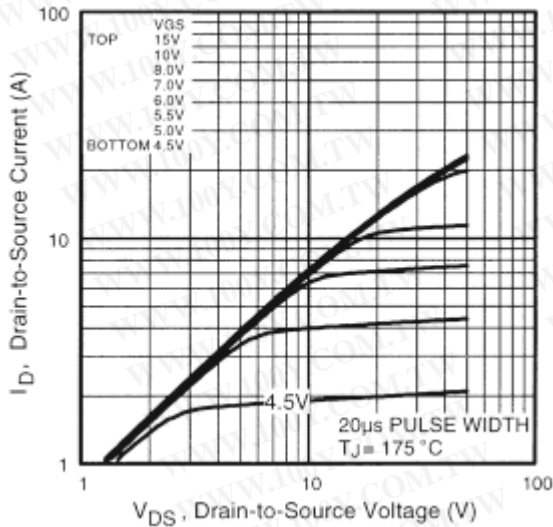


Fig. 2 - Typical Output Characteristics

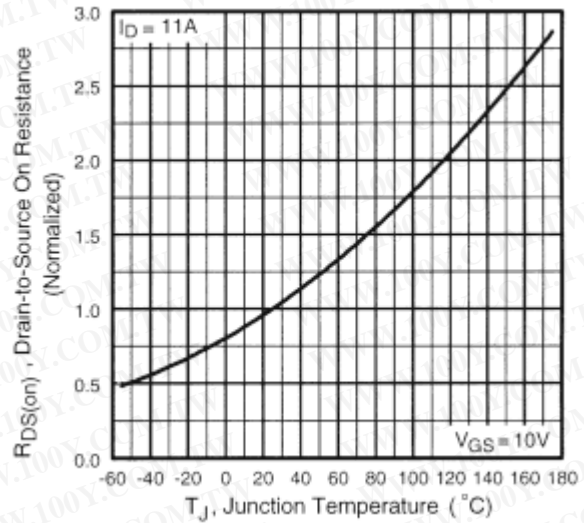


Fig. 4 - Normalized On-Resistance vs. Temperature

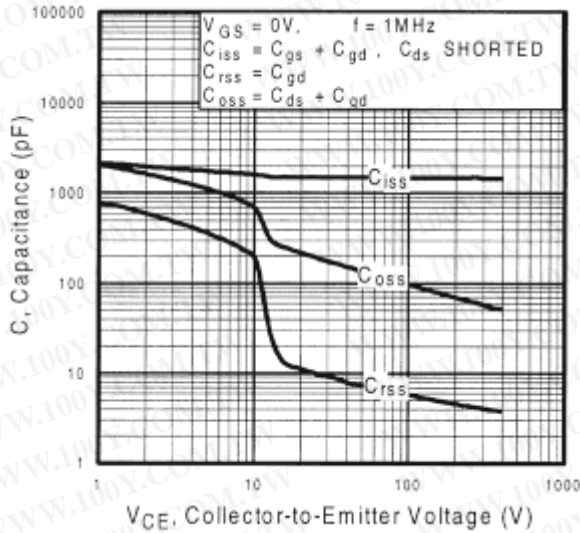


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

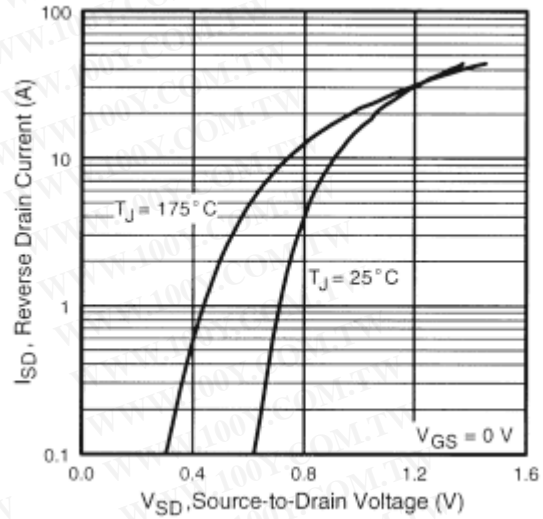


Fig. 7 - Typical Source-Drain Diode Forward Voltage

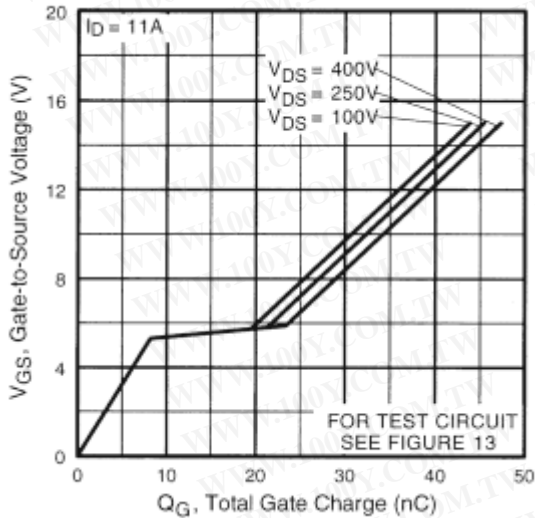


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

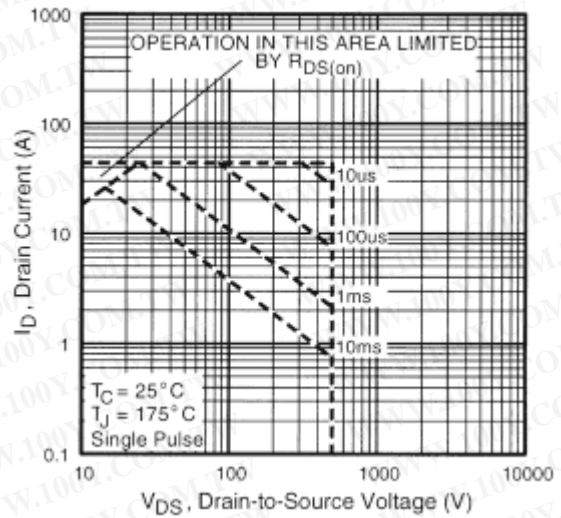


Fig. 8 - Maximum Safe Operating Area

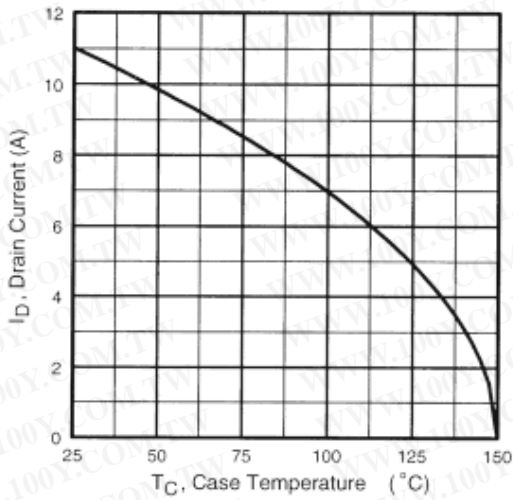


Fig. 9 - Maximum Drain Current vs. Case Temperature

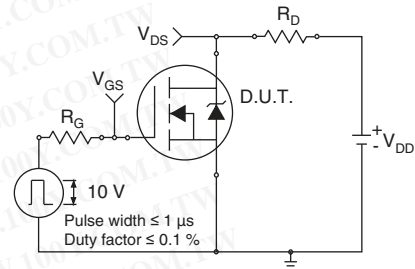


Fig. 10a - Switching Time Test Circuit

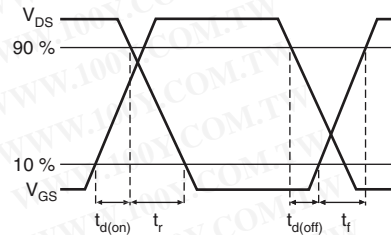


Fig. 10b - Switching Time Waveforms

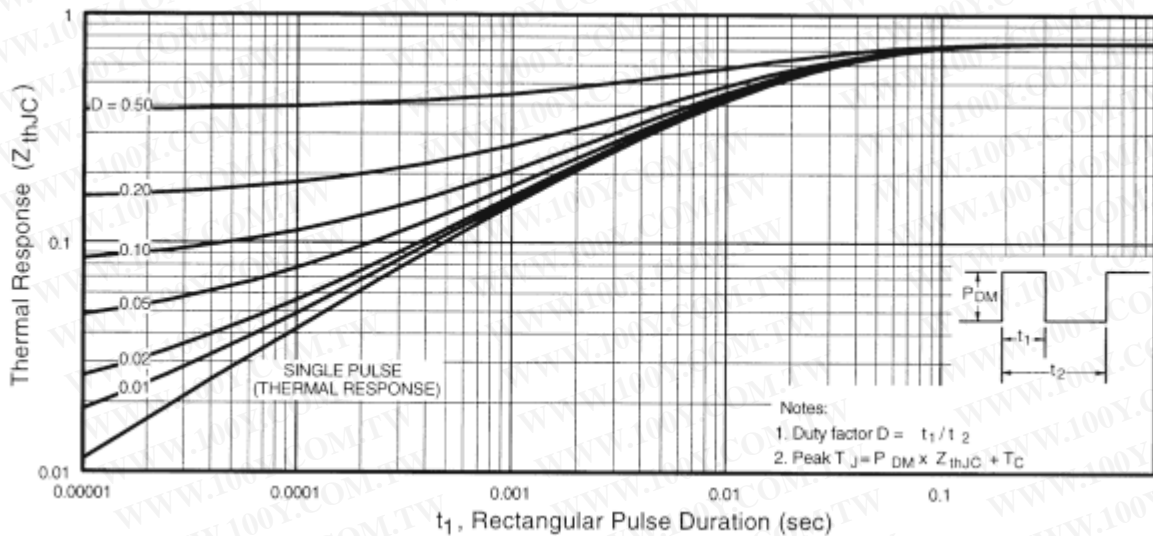


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

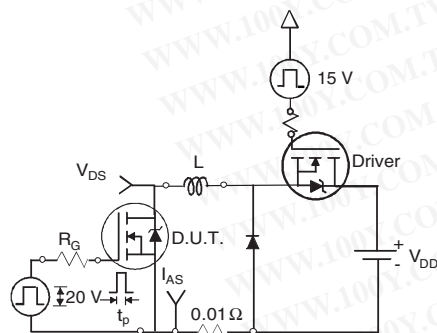


Fig. 12a - Unclamped Inductive Test Circuit

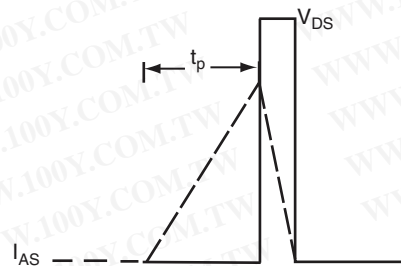


Fig. 12b - Unclamped Inductive Waveforms

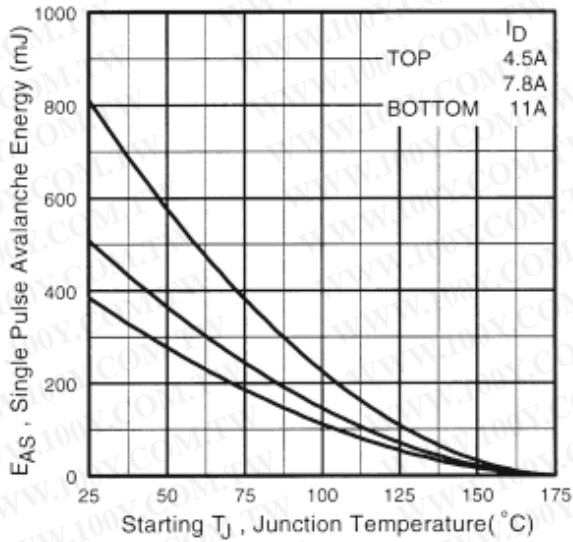


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

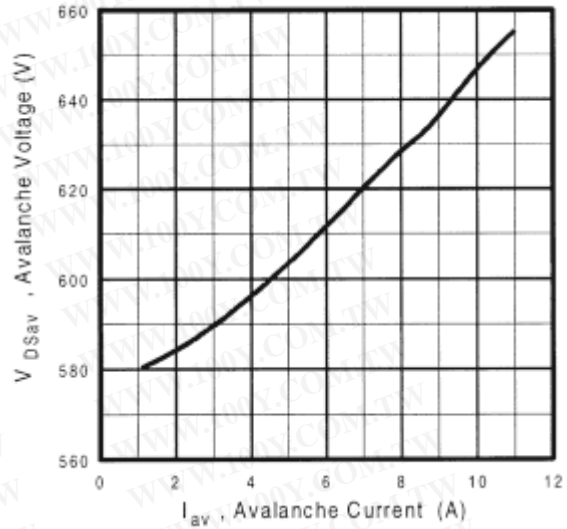


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

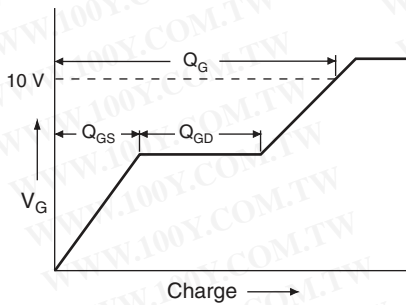


Fig. 13a - Basic Gate Charge Waveform

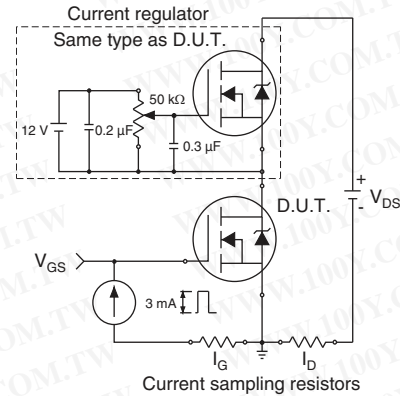
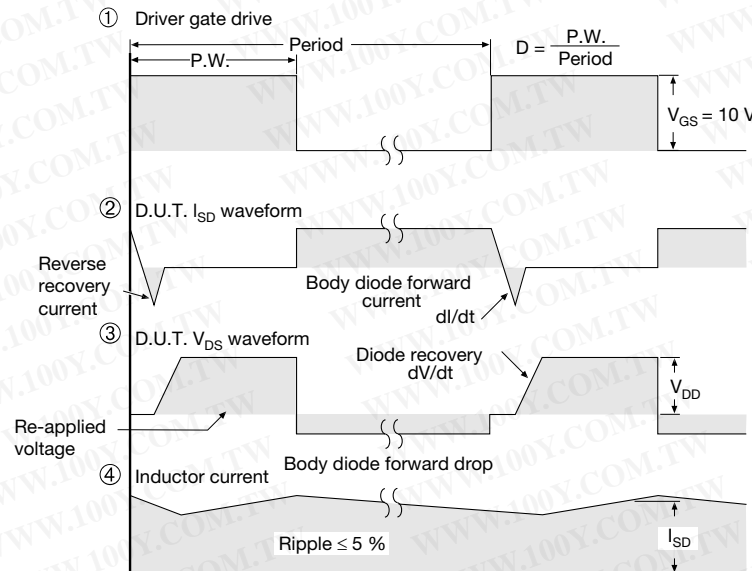
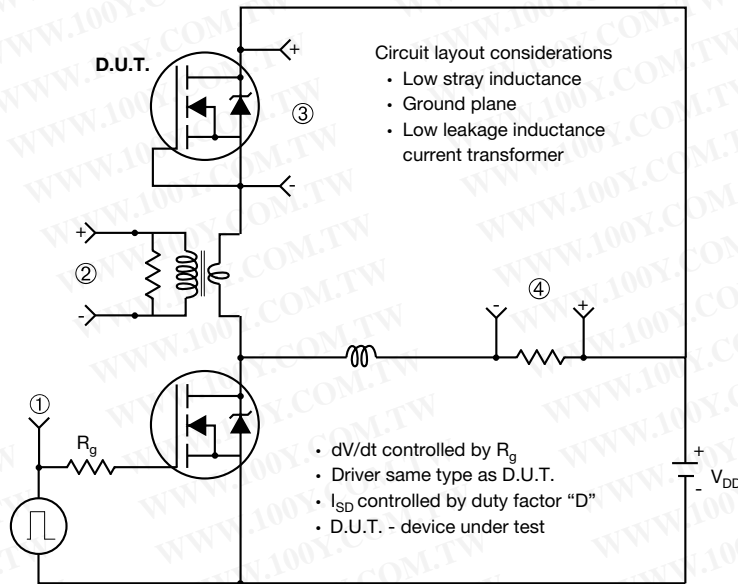


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



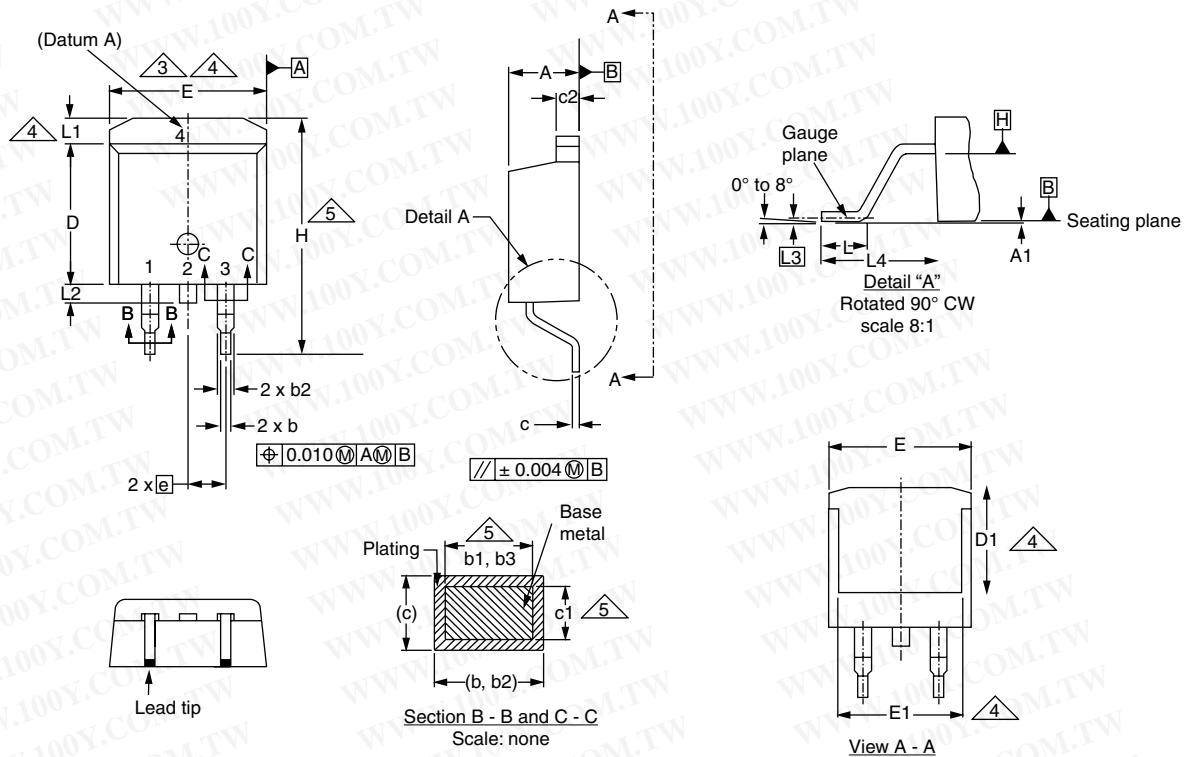
Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 11 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



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