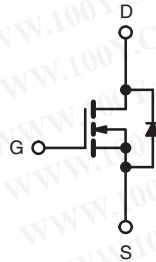
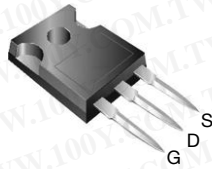


勝特力材料 886-3-5753170
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Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	500
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.190
Q_g (Max.) (nC)	150
Q_{gs} (nC)	44
Q_{gd} (nC)	72
Configuration	Single

TO-247AC



N-Channel MOSFET

FEATURES

- Superfast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhanced dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFP23N50LPbF
	SiHFP23N50L-E3
SnPb	IRFP23N50L
	SiHFP23N50L


ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	500	V	
Gate-Source Voltage	V_{GS}	± 30		
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	23	A
		$T_C = 100\text{ }^\circ\text{C}$	15	
Pulsed Drain Current ^a	I_{DM}	92		
Linear Derating Factor		2.9	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy ^b	E_{AS}	410	mJ	
Repetitive Avalanche Current ^a	I_{AR}	23	A	
Repetitive Avalanche Energy ^a	E_{AR}	37	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	370	W
Peak Diode Recovery dV/dt^c		dV/dt	21	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d	
Mounting Torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.5\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 23\text{ A}$ (see fig. 12).
- $I_{SD} \leq 23\text{ A}$, $dI/dt \leq 650\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.34	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^d$	-	0.27	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	μA
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	2.0	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 14\text{ A}^b$	-	0.190	0.235	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 14\text{ A}^b$	12	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	3600	-	pF
Output Capacitance	C_{oss}		-	380	-	
Reverse Transfer Capacitance	C_{rss}		-	37	-	
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	4800	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	100	-
Effective Output Capacitance (Energy Related)	$C_{oss\text{ eff. (ER)}}$		$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	220	-
			$V_{DS} = 0\text{ V to } 400\text{ V}^d$	-	160	-
Internal Gate Resistance	R_G	$f = 1\text{ MHz}$, open drain	-	1.2	-	Ω
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 23\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 ^b	-	-	150	nC
Gate-Source Charge	Q_{gs}		-	-	44	
Gate-Drain Charge	Q_{gd}		-	-	72	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 23\text{ A}, R_G = 6.0, V_{GS} = 10\text{ V}$ see fig. 10 ^b	-	26	-	ns
Rise Time	t_r		-	94	-	
Turn-Off Delay Time	$t_{d(off)}$		-	53	-	
Fall Time	t_f		-	45	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	23	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	92	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 14\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$	-	170	250	ns
		$T_J = 125\text{ }^\circ\text{C}$	-	220	330	
Body Diode Reverse Recovery Charge	Q_{rr}	$T_J = 25\text{ }^\circ\text{C}$	-	560	840	μC
		$T_J = 125\text{ }^\circ\text{C}$	-	980	1500	
Reverse Recovery Current	I_{RRM}	$T_J = 25\text{ }^\circ\text{C}$	-	7.6	11	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
- $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

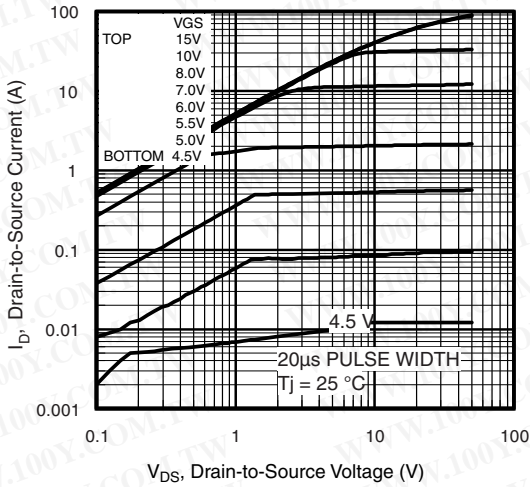


Fig. 1 - Typical Output Characteristics

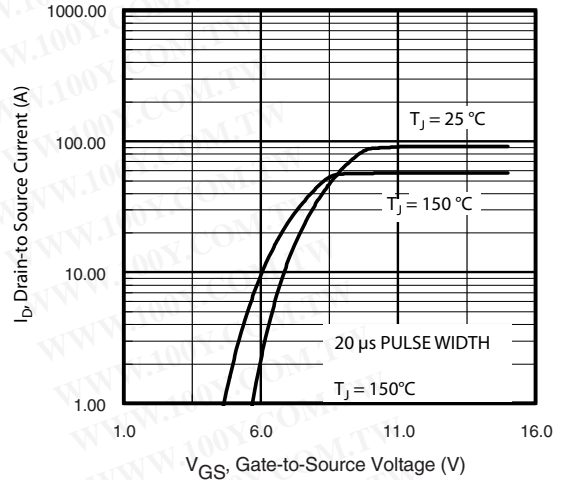


Fig. 3 - Typical Transfer Characteristics

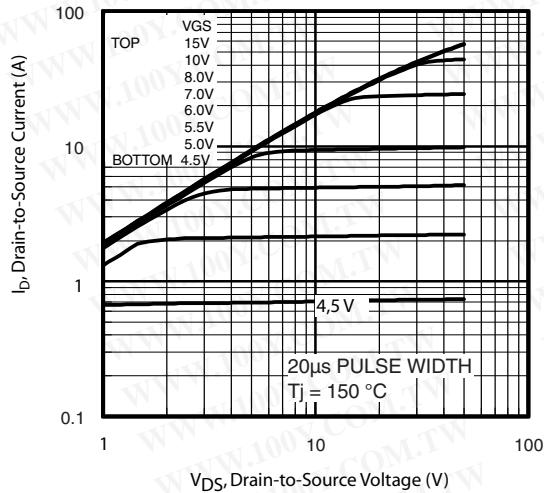


Fig. 2 - Typical Output Characteristics

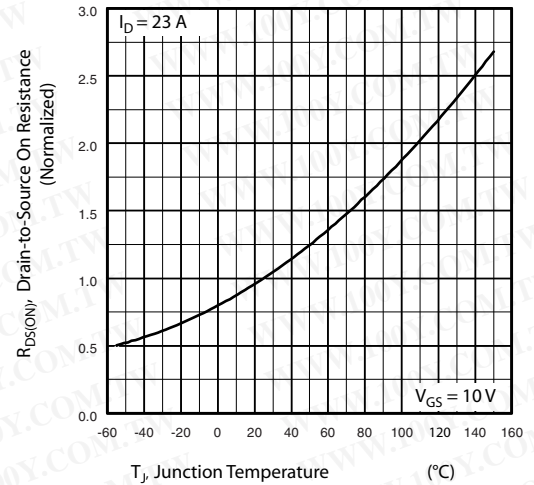


Fig. 4 - Normalized On-Resistance vs. Temperature

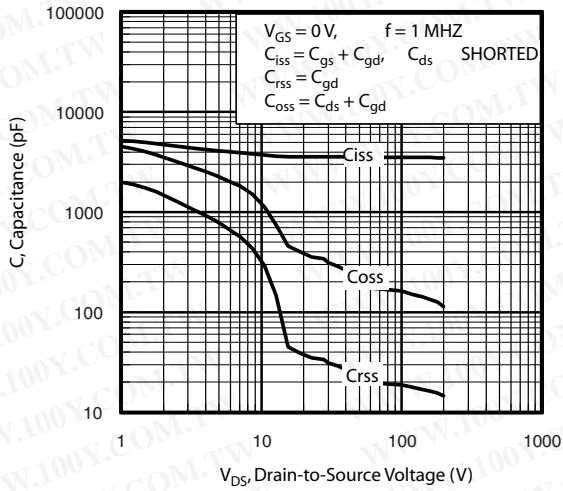


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

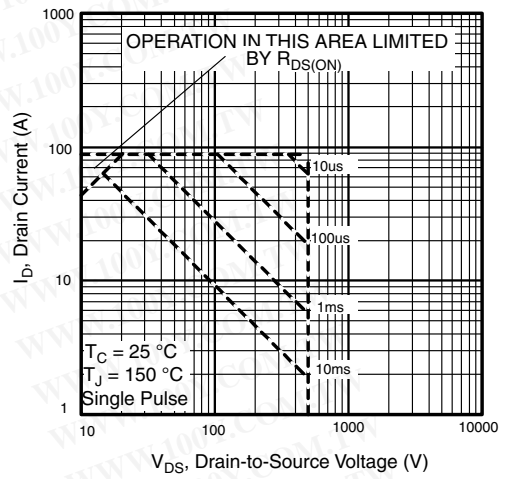


Fig. 7 - Maximum Safe Operating Area

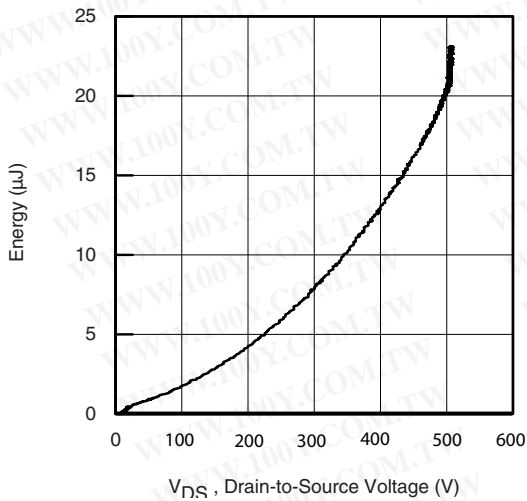


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

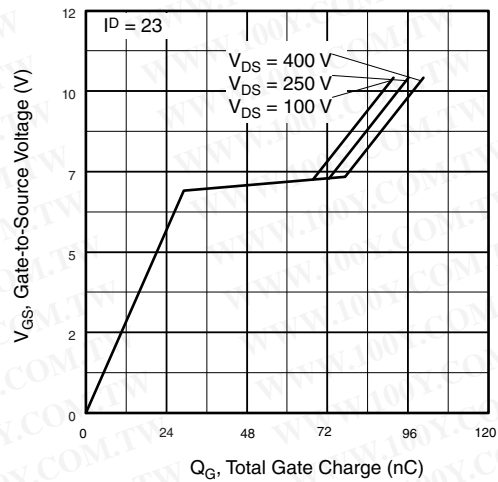


Fig. 8 - Typical Gate Charge vs. Gate-to-Source Voltage

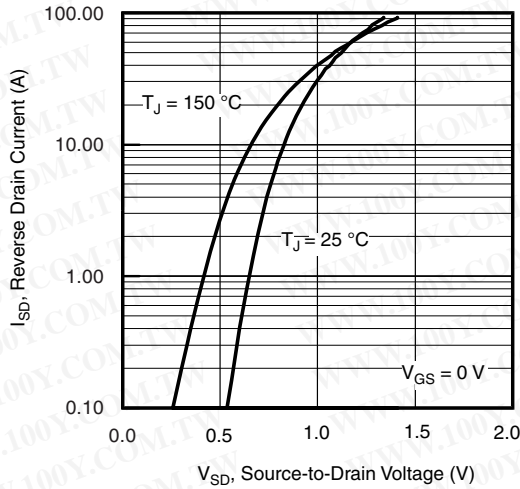


Fig. 9 - Typical Source-Drain Diode Forward Voltage

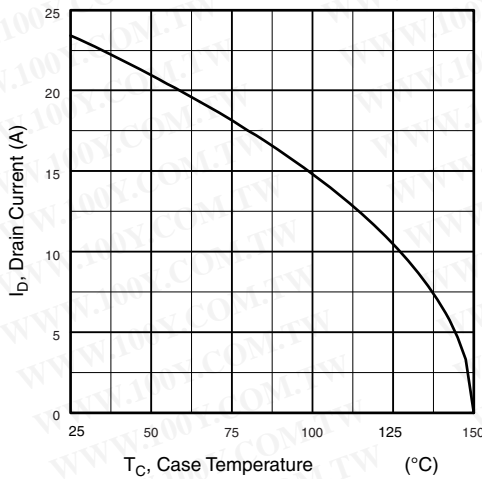


Fig. 10 - Maximum Drain Current vs. Case Temperature

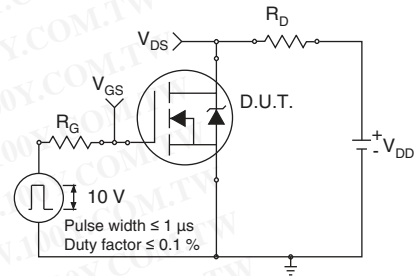


Fig. 11a - Switching Time Test Circuit

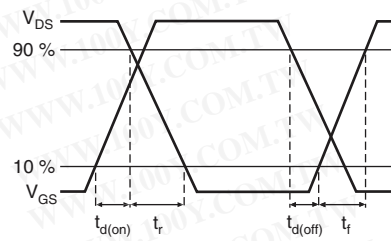


Fig. 11b - Switching Time Waveforms

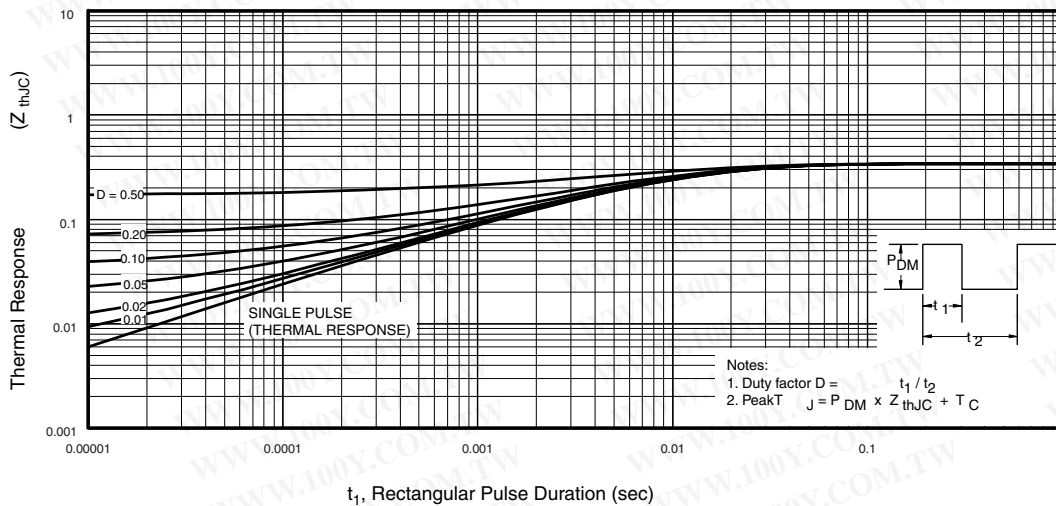


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

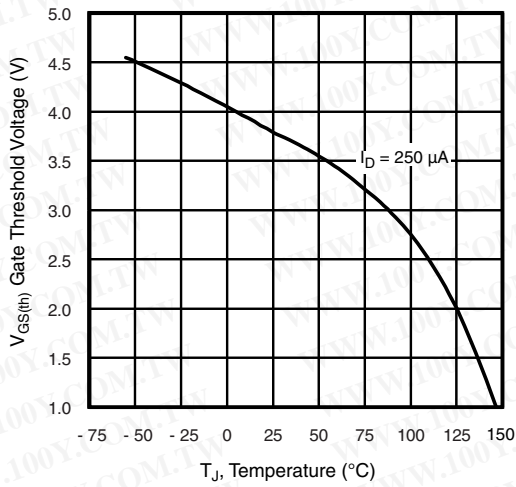


Fig. 13 - Threshold Voltage vs. Temperature

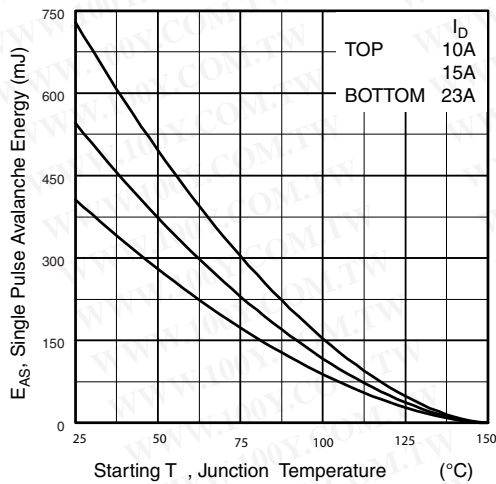


Fig. 14 - Maximum Avalanche Energy s. Drain Current

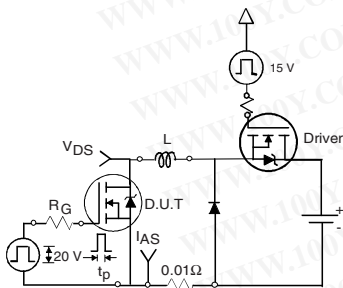


Fig. 15a - Unclamped Inductive Test Circuit

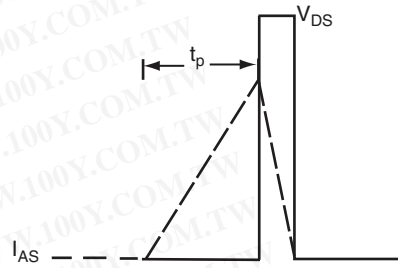


Fig. 15b - Unclamped Inductive Waveforms

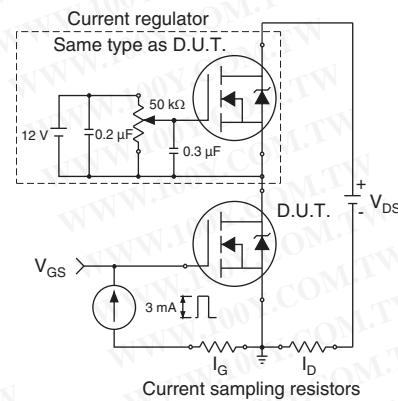


Fig. 16a - Gate Charge Test Circuit

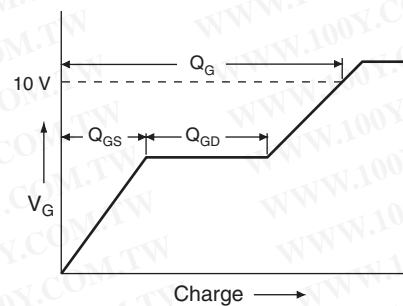
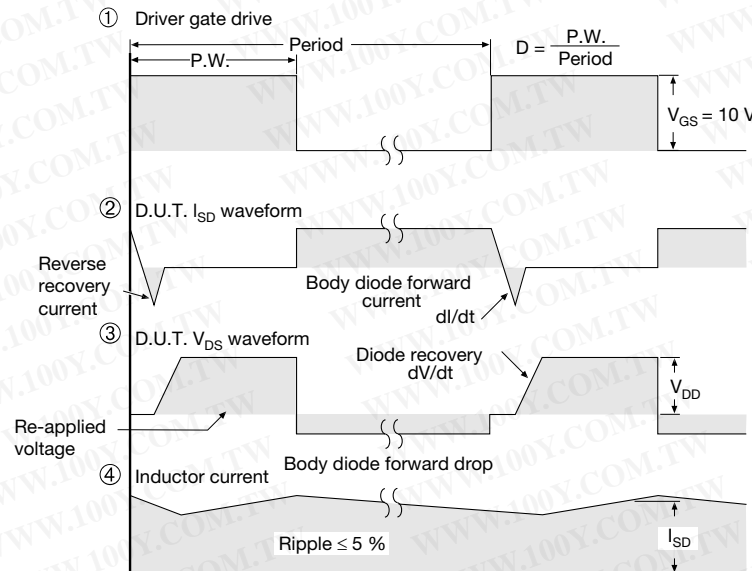
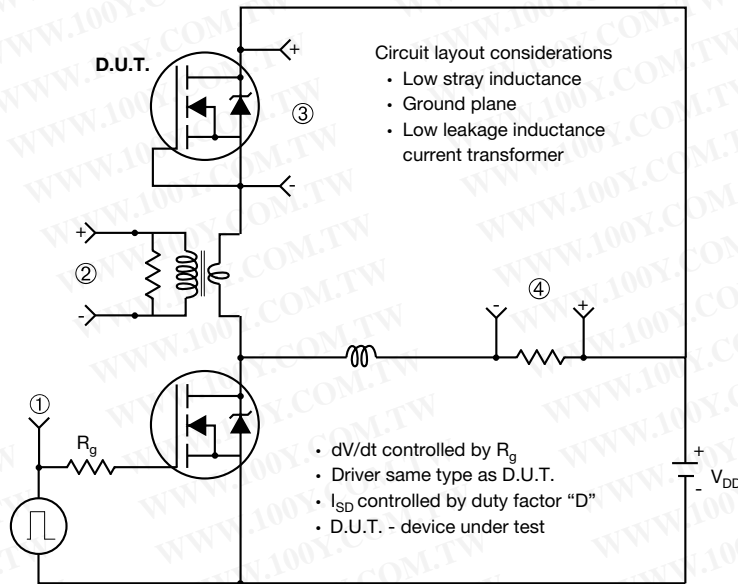


Fig. 16b - Basic Gate Charge Waveform

Peak Diode Recovery dV/dt Test Circuit



Note

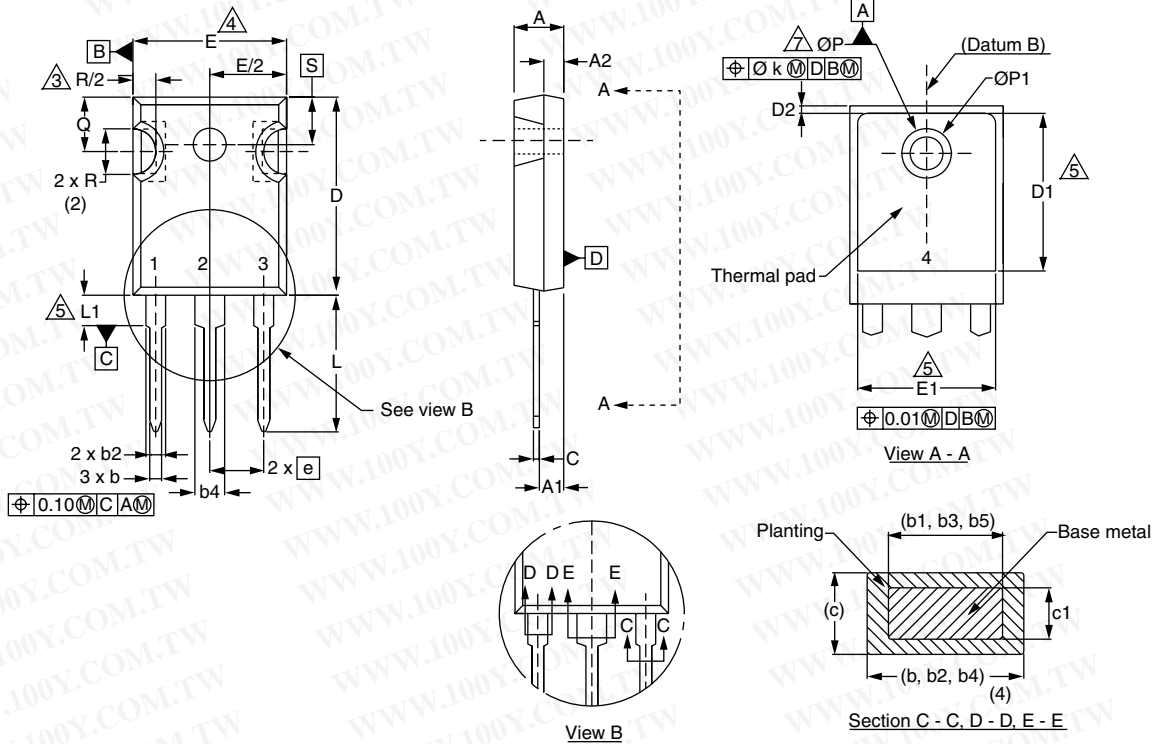
a. $V_{GS} = 5 V$ for logic level devices

Fig. 17 - For N-Channel

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TO-247AC (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.65	5.31	0.183	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.65	2.39	0.065	0.094
b3	1.65	2.37	0.065	0.093
b4	2.59	3.43	0.102	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.70	0.776	0.815
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
ϕk	0.254		0.010	
L	14.20	16.10	0.559	0.634
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
ϕP	3.56	3.66	0.140	0.144
$\phi P1$	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: S-81920-Rev. A, 15-Sep-08
DWG: 5971

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. ϕP to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.



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