

TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type ( $\pi$ -MOSV)

# 2SK2865

Chopper Regulator, DC/DC Converter and Motor Drive Applications

- Low drain-source ON-resistance :  $R_{DS(ON)} = 4.2 \Omega$  (typ.)
- High forward transfer admittance :  $|Y_{fs}| = 1.7 \text{ S}$  (typ.)
- Low leakage current :  $I_{DSS} = 100 \mu\text{A}$  (max) ( $V_{DS} = 600 \text{ V}$ )
- Enhancement mode :  $V_{th} = 2.0 \text{ to } 4.0 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 1 \text{ mA}$ )

## Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristic		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	600	V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )		$V_{DGR}$	600	V
Gate-source voltage		$V_{GSS}$	$\pm 30$	V
Drain current	DC (Note 1)	$I_D$	2	A
	Pulse ( $t = 1 \text{ ms}$ ) (Note 1)	$I_{DP}$	5	A
	Pulse ( $t = 100 \mu\text{s}$ ) (Note 1)	$I_{DP}$	8	A
Drain power dissipation ( $T_c = 25^\circ\text{C}$ )		$P_D$	20	W
Single-pulse avalanche energy (Note 2)		$E_{AS}$	93	mJ
Avalanche current		$I_{AR}$	2	A
Repetitive avalanche energy (Note 3)		$E_{AR}$	2	mJ
Channel temperature		$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range		$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	6.25	$^\circ\text{C} / \text{W}$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	125	$^\circ\text{C} / \text{W}$

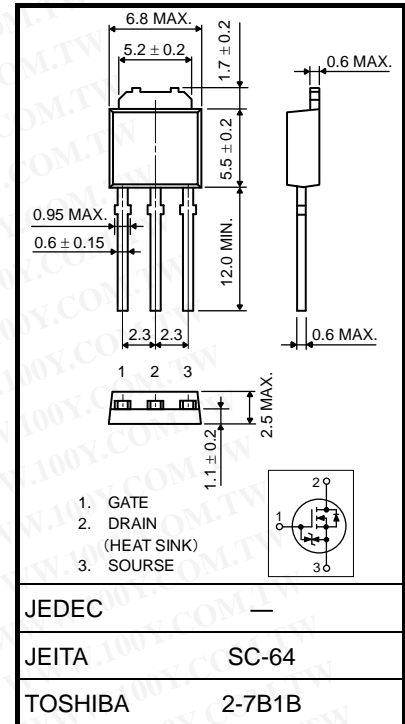
Note 1: Ensure that the channel temperature does not exceed  $150^\circ\text{C}$ .

Note 2:  $V_{DD} = 90 \text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$  (initial),  $L = 41 \text{ mH}$ ,  $R_G = 25 \Omega$ ,  $I_{AR} = 2 \text{ A}$

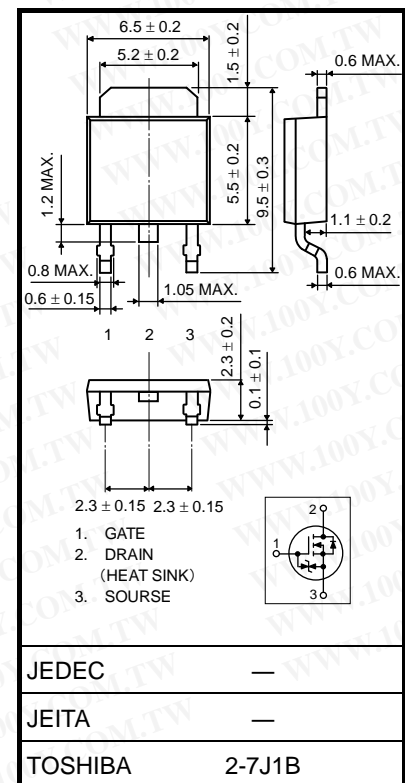
Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.

Unit: mm



Weight: 0.36 g (typ.)



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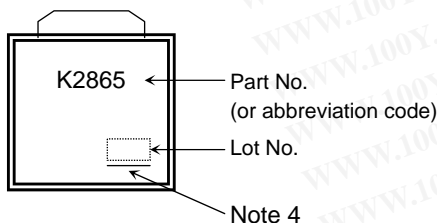
## Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I <sub>GSS</sub>	V <sub>GS</sub> = ±25 V, V <sub>DS</sub> = 0 V	—	—	±10	μA
Gate-source breakdown voltage		V <sub>(BR) GSS</sub>	I <sub>G</sub> = ±10 μA, V <sub>DS</sub> = 0 V	±30	—	—	V
Drain cutoff current		I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	—	—	100	μA
Drain-source breakdown voltage		V <sub>(BR) DSS</sub>	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	600	—	—	V
Gate threshold voltage		V <sub>th</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	2.0	—	4.0	V
Drain-source ON-resistance		R <sub>DS (ON)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1 A	—	4.2	5.0	Ω
Forward transfer admittance		Y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 A	0.8	1.7	—	S
Input capacitance		C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	—	380	—	pF
Reverse transfer capacitance		C <sub>rss</sub>		—	40	—	
Output capacitance		C <sub>oss</sub>		—	120	—	
Switching time	Rise time	t <sub>r</sub>		—	15	—	ns
	Turn-on time	t <sub>on</sub>		—	25	—	
	Fall time	t <sub>f</sub>		—	20	—	
	Turn-off time	t <sub>off</sub>		—	80	—	
Total gate charge (gate-source plus gate-drain)		Q <sub>g</sub>	V <sub>DD</sub> ≈ 480 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2 A	—	9	—	nC
Gate-source charge		Q <sub>gs</sub>		—	5	—	
Gate-drain ("Miller") charge		Q <sub>gd</sub>		—	4	—	

## Source-Drain Ratings and Characteristics (Ta = 25°C)

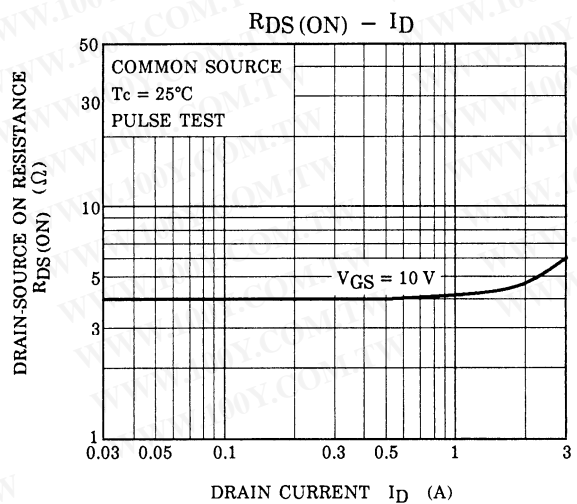
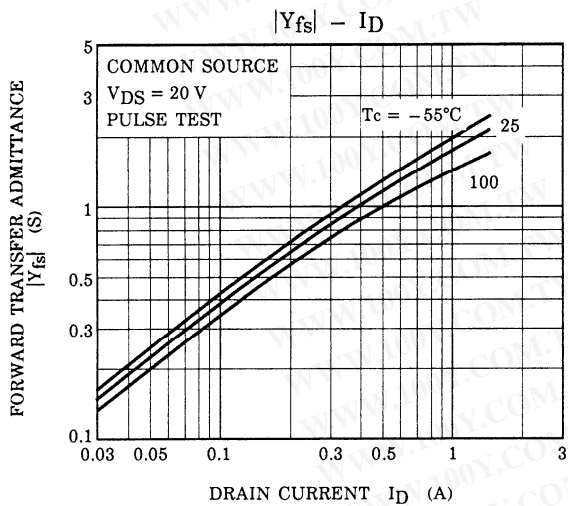
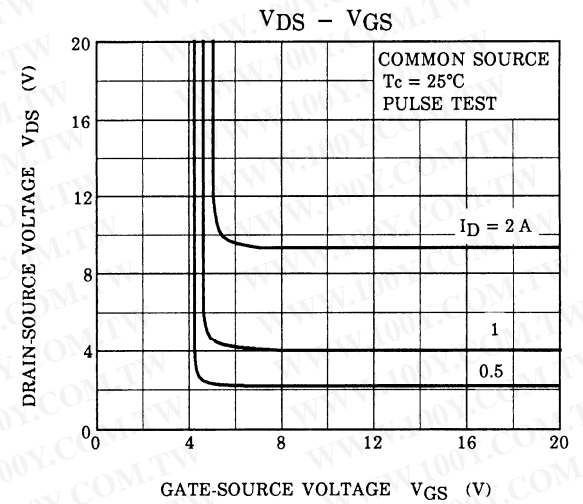
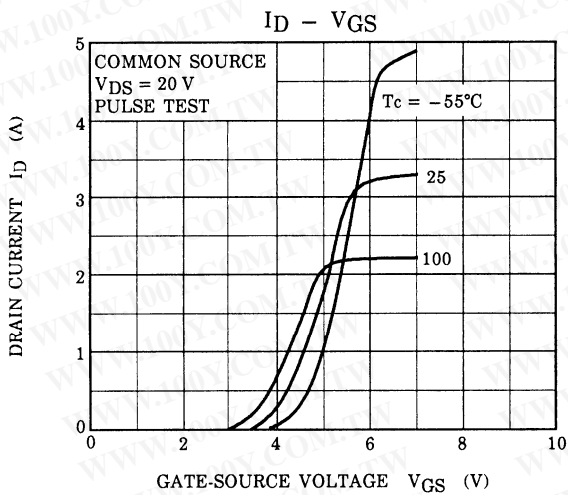
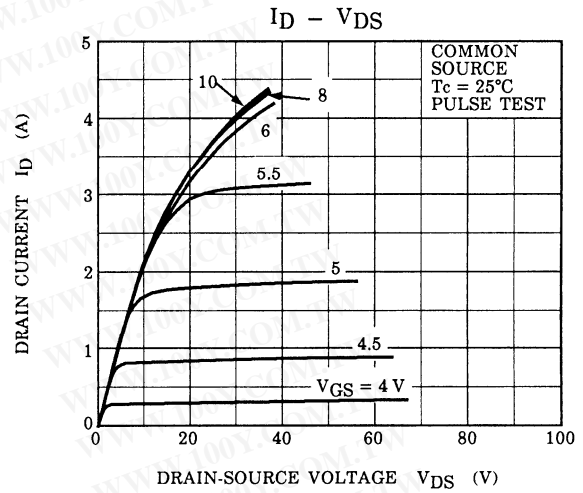
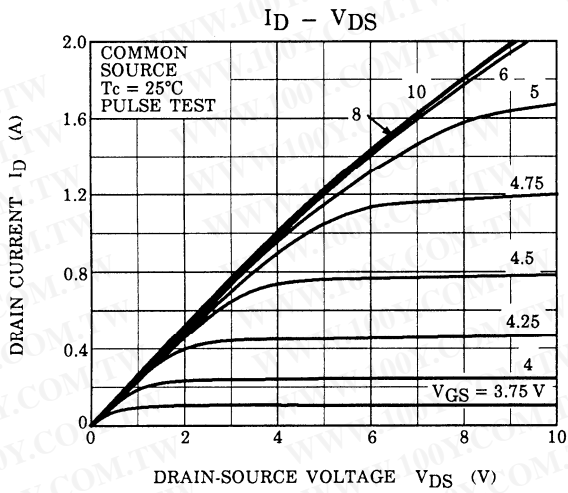
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I <sub>DR</sub>	—	—	—	2	A
Pulse drain reverse current (Note 1)	I <sub>DRP</sub>	t = 1 ms	—	—	5	A
	I <sub>DRP</sub>	t = 100 μs	—	—	8	A
Forward voltage (diode)	V <sub>DSF</sub>	I <sub>DR</sub> = 2 A, V <sub>GS</sub> = 0 V	—	—	-1.5	V
Reverse recovery time	t <sub>rr</sub>	I <sub>DR</sub> = 2 A, V <sub>GS</sub> = 0 V	—	1000	—	ns
Reverse recovery charge	Q <sub>rr</sub>	dI <sub>DR</sub> / dt = 100 A/μs	—	3.5	—	μC

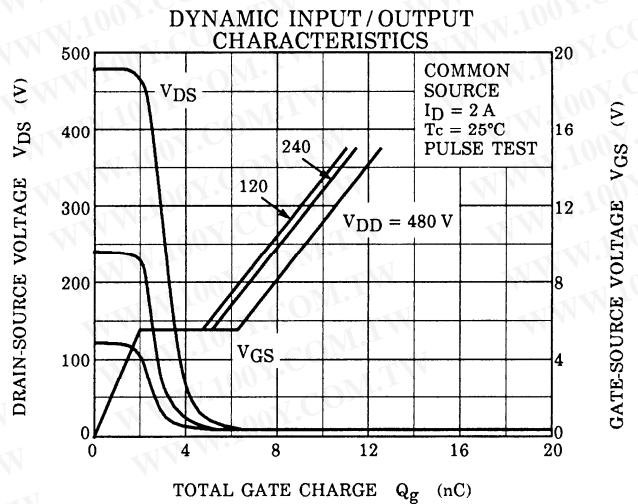
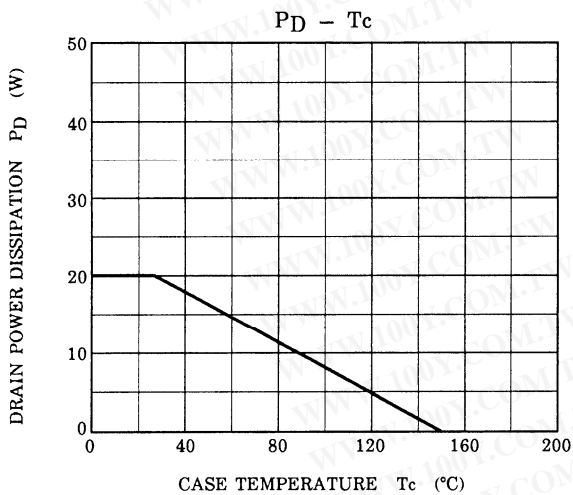
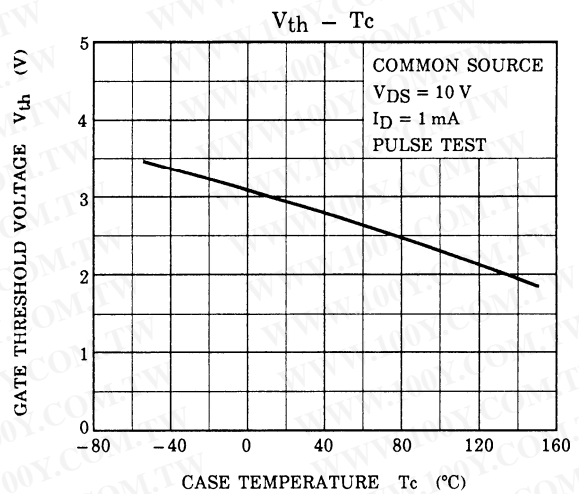
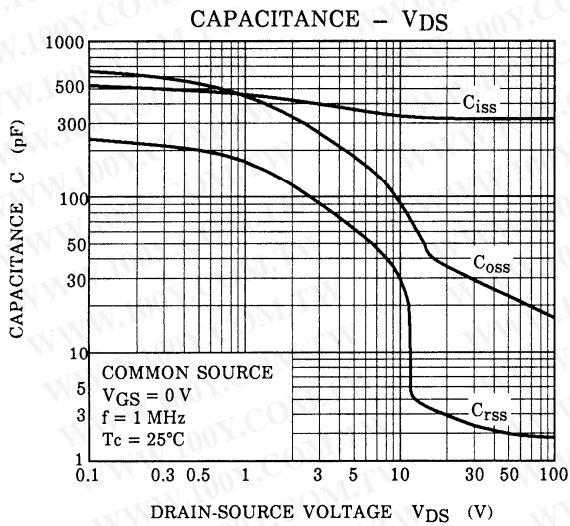
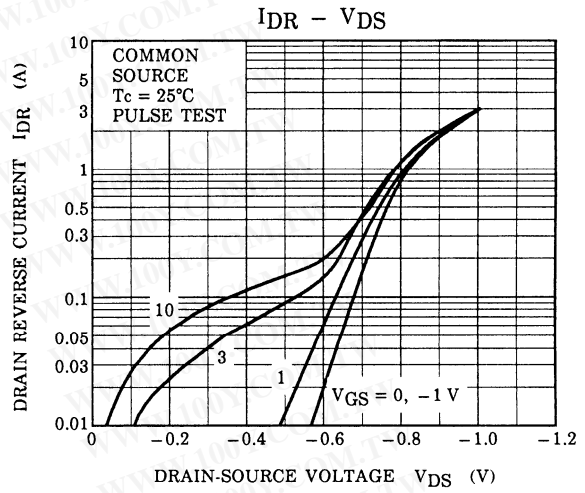
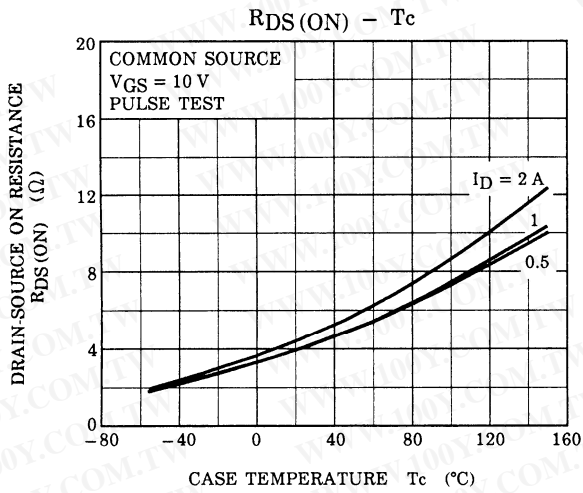
## Marking

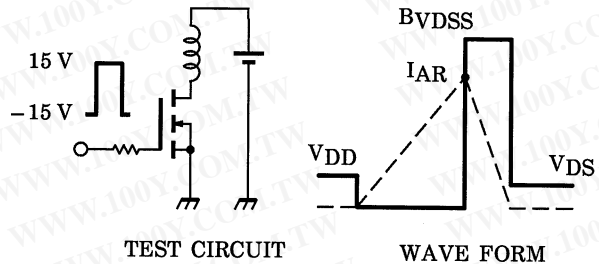
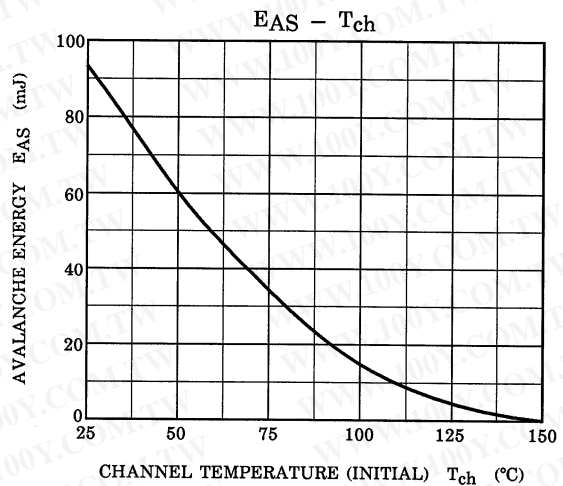
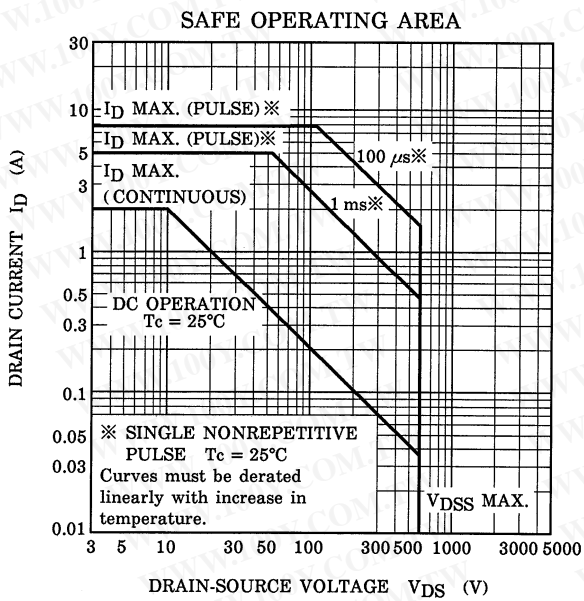
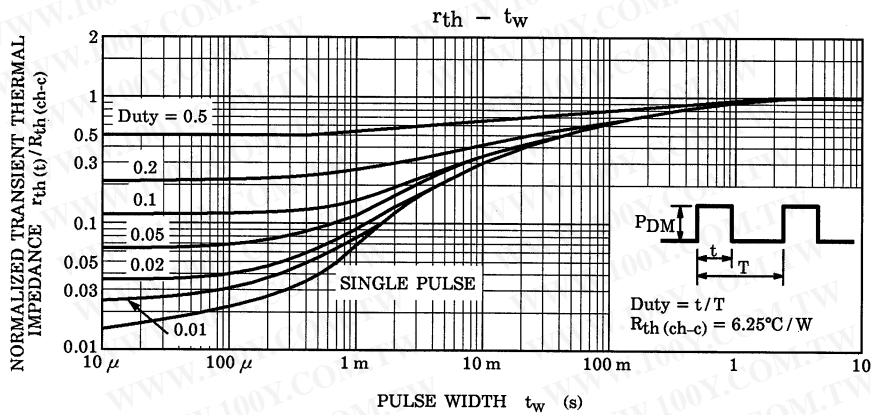


Note 4 : A line under a Lot No. identifies the indication of product Labels [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.







$R_G = 25 \Omega$   
 $V_{DD} = 90 V, L = 41 mH$

$$EAS = \frac{1}{2} \cdot L \cdot I^2 \cdot \left( \frac{BVDSS}{BVDSS - V_{DD}} \right)$$

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# Transistors: DP Package

In developing your designs, please ensure the datasheet.

Specification of DP package	
JEITA	-
Mounting	Through Hole
Pins	3
Weight (typ.)	0.36g
Packing Name	-
Packing Method	-
Minimum Quantity	-
Package Dimensions(mm)	<p>The diagram illustrates the mechanical specifications of the DP package. It includes three views: a top view, a side view, and a bottom view. The top view shows a rectangular body with a width of 6.8 mm (maximum) and a height of 7.2 mm. Three pins extend from the bottom of the body, with a pin-to-pin pitch of 2.3 mm and a pin diameter of 0.6 mm. The maximum length of the pins is 12.0 mm. The side view shows a maximum body thickness of 2.5 mm and a maximum pin diameter of 0.6 mm. The bottom view shows three rectangular pads, each 0.95 mm wide, corresponding to the pins.</p>

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# Transistors: New PW-Mold Package

In developing your designs, please ensure the datasheet.

Specification of New PW-Mold package	
JEITA	-
Mounting	Surface Mount
Pins	3
Weight (typ.)	0.36g
Packing Name	TE16L1
Packing Method	Embossed Tape
Minimum Quantity	2,000pcs/Reel
Tape Width (mm)	16
Package Dimensions(mm) / Land Pattern Example(mm)	
Tape Dimensions(mm) / Reel Dimensions(mm)	

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