STN4NF03L

N-channel 30 V - 0.039 Ω - 6.5 A - SOT-223 STripFET™ II Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STN4NF03L	30 V	<0.05 Ω	6.5 A

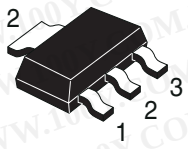
- Low threshold drive

Application

- Switching applications

Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.



SOT-223

Figure 1. Internal schematic diagram

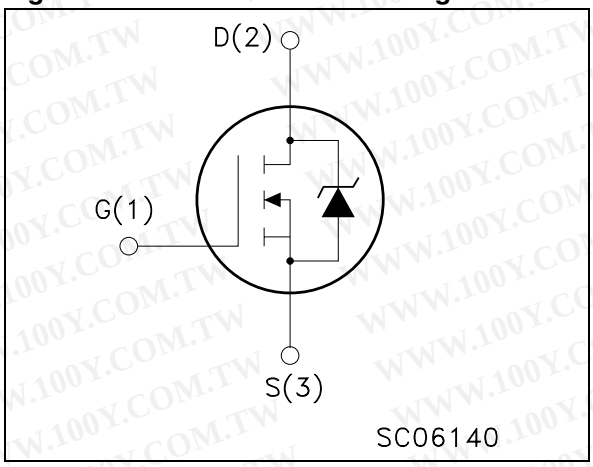


Table 1. Device summary

Order code	Marking	Package	Packaging
STN4NF03L	4NF03L	SOT-223	Tape & reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-source voltage	± 16	V
I_D	Drain current (continuous) at T_C = 25 °C	6.5	A
I_D	Drain current (continuous) at T_C=100 °C	4.5	A
I_{DM} (1)	Drain current (pulsed)	26	A
P_{TOT}	Total dissipation at T_C = 25 °C	3.3	W
	Derating factor	0.026	W/°C
E_{AS} (2)	Single pulse avalanche energy	100	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area
2. Starting T_J = 25 °C, I_D = 6 A

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-pcb	Thermal resistance junction-PCB(1) max	38	°C/W
Rthj-pcb	Thermal resistance junction-PCB(2) max	100	°C/W
T_l	Maximum lead temperature for soldering purpose (for 10 sec. 1.6 mm from case) typ	260	°C

1. When mounted on 1 inch^2 FR-4 board, 2 oz. Cu., t < 10 s
2. Minimum recommended footprint

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating, V_{DS} = max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±16 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2 A V_{GS} = 5 V, I_D= 2 A		0.039 0.046	0.05 0.06	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 10 V, I_D = 1 A	3	6		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f=1 MHz, V_{GS} = 0		330 90 40		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}= 24 V, I_D = 4 A V_{GS} =10 V *(see Figure 14)*		6.5 3.2 2	9	nC nC nC

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time rise time	V_{DD} = 15 V, I_D= 2 A, R_G = 4.7 Ω, V_{GS} = 4.5 V *(see Figure 15)*		11 100		ns ns
$t_{d(off)}$ t_f	Turn-off-delay time fall time	V_{DD} = 15 V, I_D = 2 A, R_G = 4.7 Ω, V_{GS} = 4.5 V *(see Figure 15)*		35 22		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				6.5	A
I_{SDM} (1)	Source-drain current (pulsed)				26	A
V_{SD} (2)	Forward on voltage	I_{SD} = 6.5 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 6.5 A, di/dt = 100 A/µs, V_{DD} = 15 V, Tj=150 °C *(see Figure 15)*		34 25 1.4		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

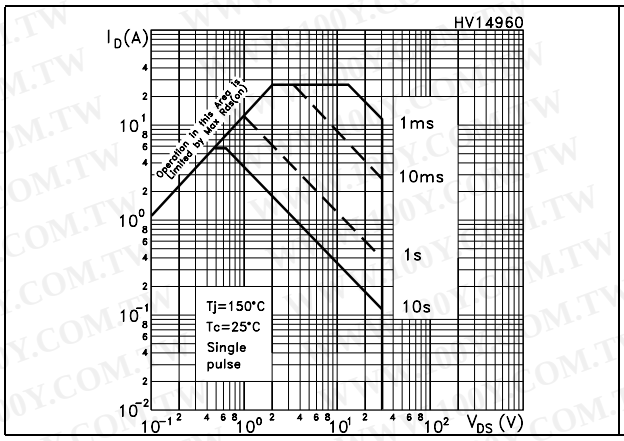


Figure 3. Thermal impedance junction-PCB

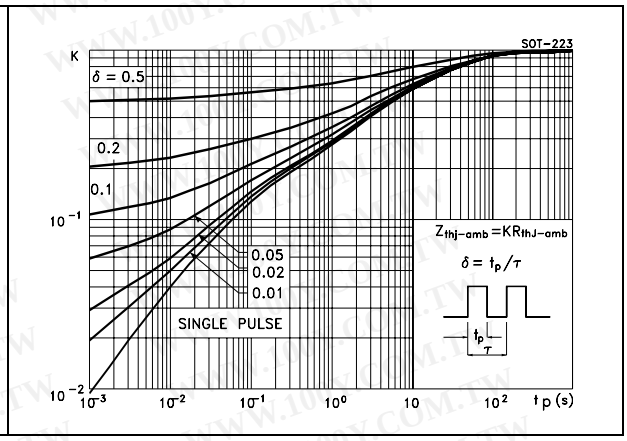


Figure 4. Output characteristics

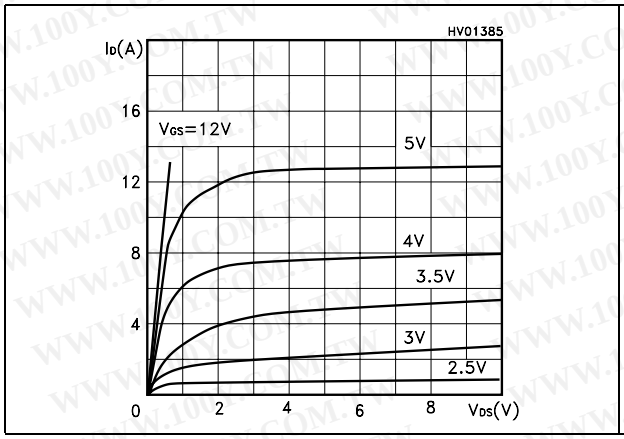


Figure 5. Transfer characteristics

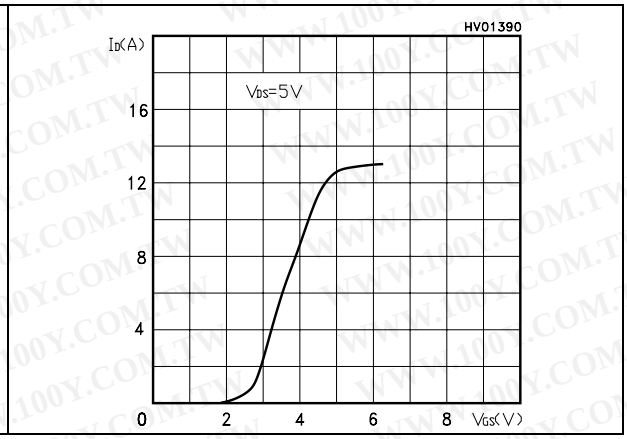


Figure 6. Transconductance

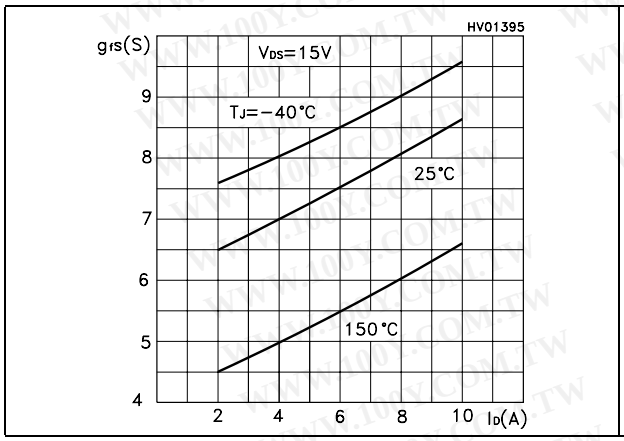


Figure 7. Static drain-source on resistance

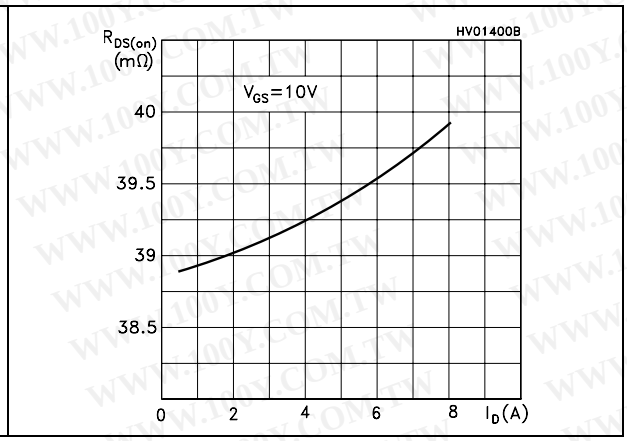


Figure 8. Gate charge vs. gate-source voltage

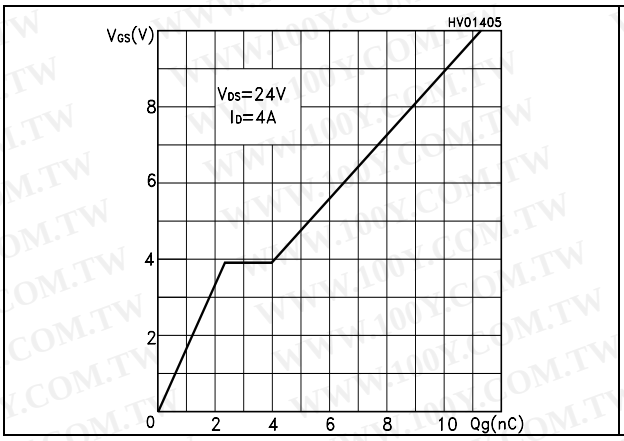


Figure 9. Capacitance variations

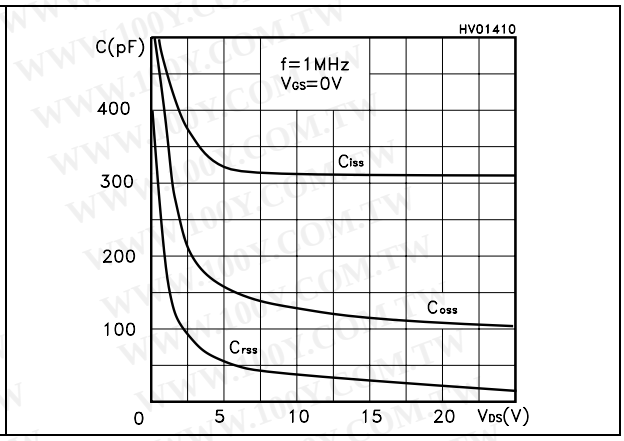


Figure 10. Normalized gate threshold voltage vs. temperature

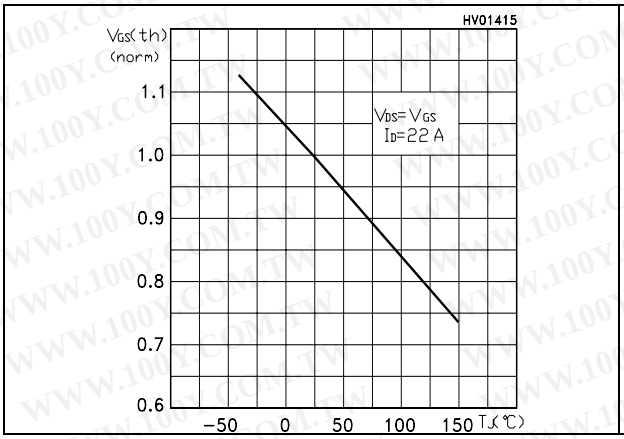


Figure 11. Normalized on resistance vs. temperature

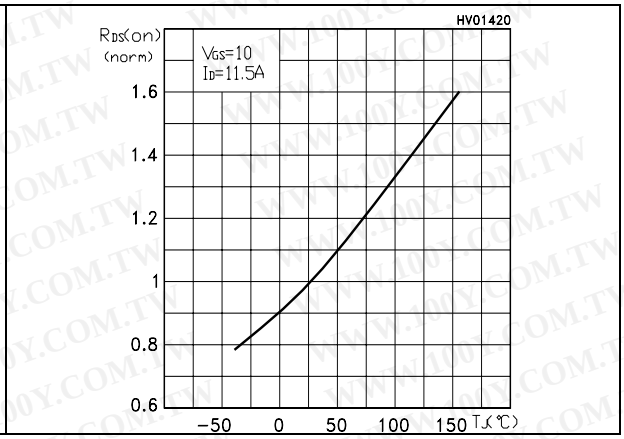
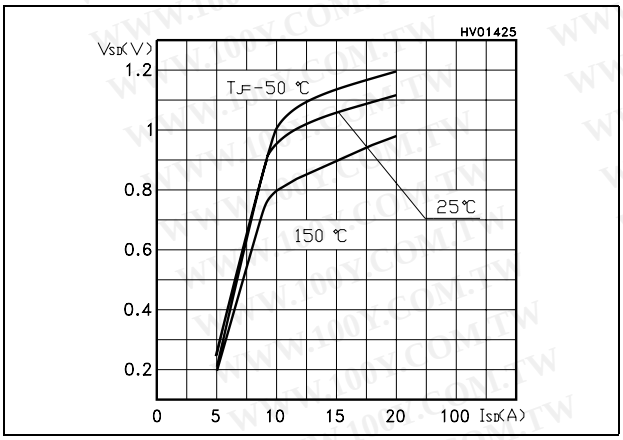


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

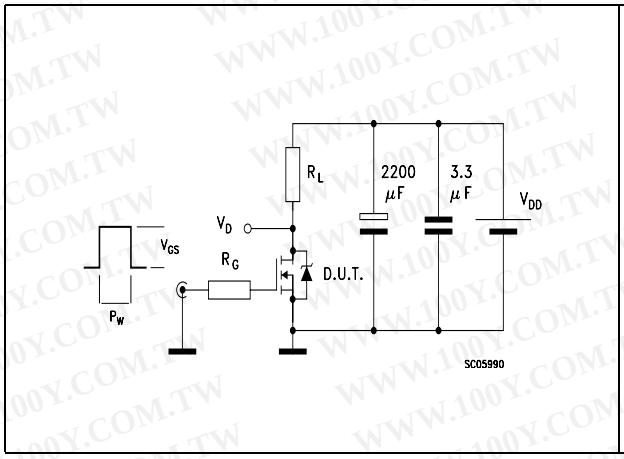


Figure 14. Gate charge test circuit

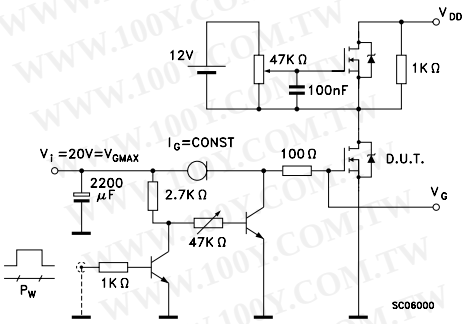


Figure 15. Test circuit for inductive load switching and diode recovery times

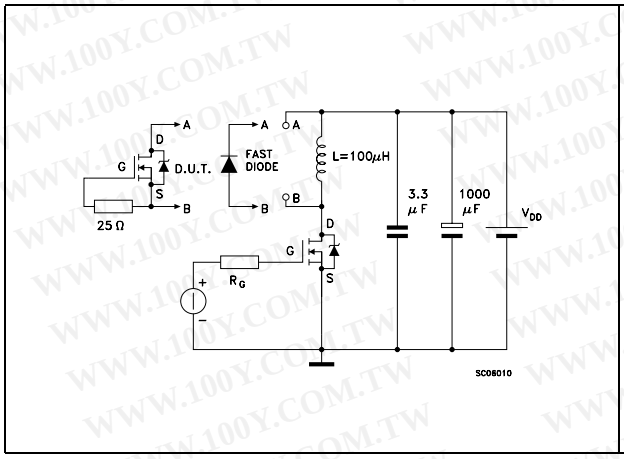


Figure 16. Unclamped inductive load test circuit

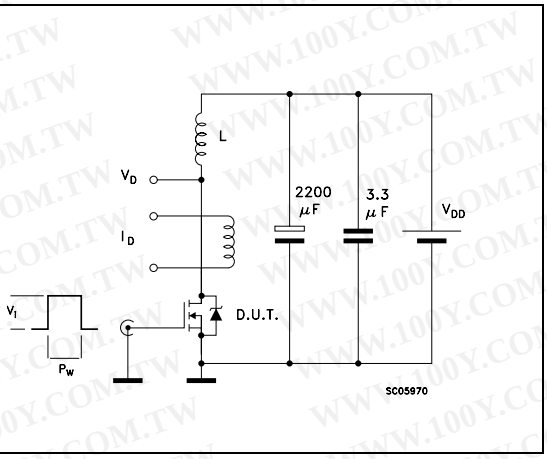


Figure 17. Unclamped inductive waveform

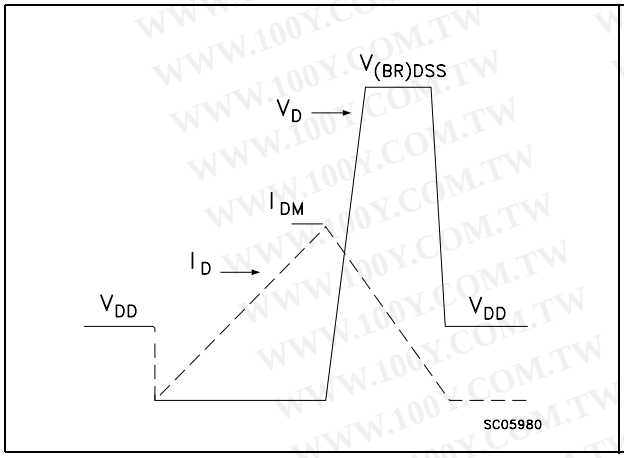
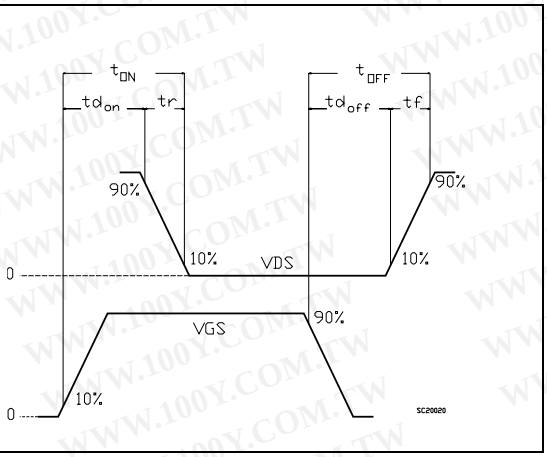


Figure 18. Switching time waveform

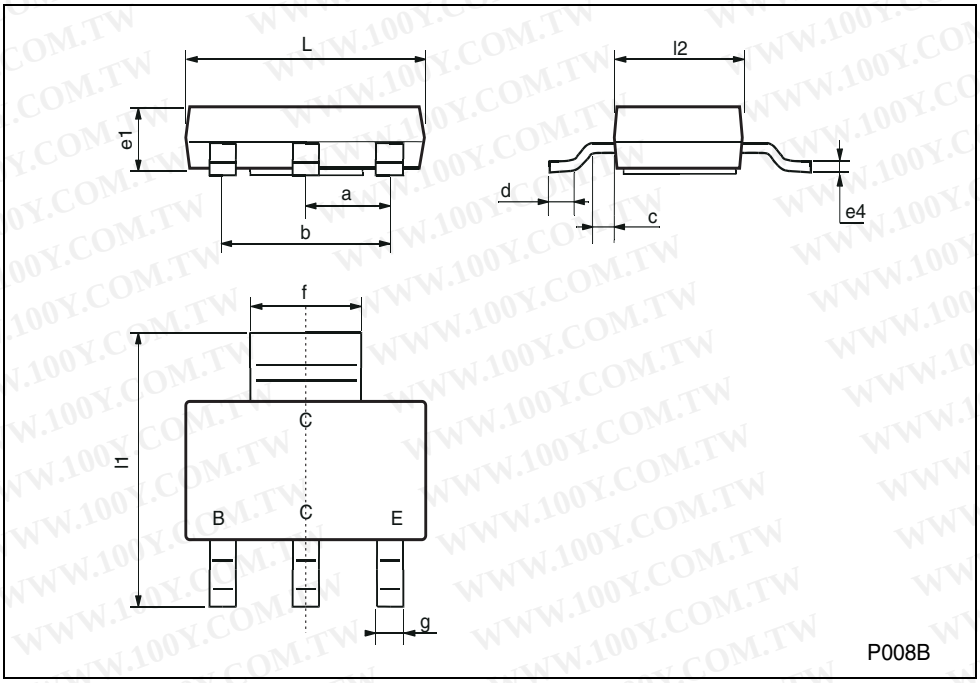


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SOT-223 MECHANICAL DATA

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a	2.27	2.3	2.33	89.4	90.6	91.7
b	4.57	4.6	4.63	179.9	181.1	182.3
c	0.2	0.4	0.6	7.9	15.7	23.6
d	0.63	0.65	0.67	24.8	25.6	26.4
e1	1.5	1.6	1.7	59.1	63	66.9
e4			0.32			12.6
f	2.9	3	3.1	114.2	118.1	122.1
g	0.67	0.7	0.73	26.4	27.6	28.7
l1	6.7	7	7.3	263.8	275.6	287.4
l2	3.5	3.5	3.7	137.8	137.8	145.7
L	6.3	6.5	6.7	248	255.9	263.8



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
21-Jun-2004	3	– Initial electronic version. – Document status promoted from preliminary data to datasheet
09-Oct-2006	4	Document reformatted no content change
27-Nov-2007	5	Updated marking on *Table 1: Device summary*
11-Dec-2007	6	Updated E_{AS} value on *Table 2: Absolute maximum ratings*

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