



## STN2NF10

N-channel 100V - 0.23Ω - 2.4A - SOT-223  
STripFET™ II Power MOSFET

### Features

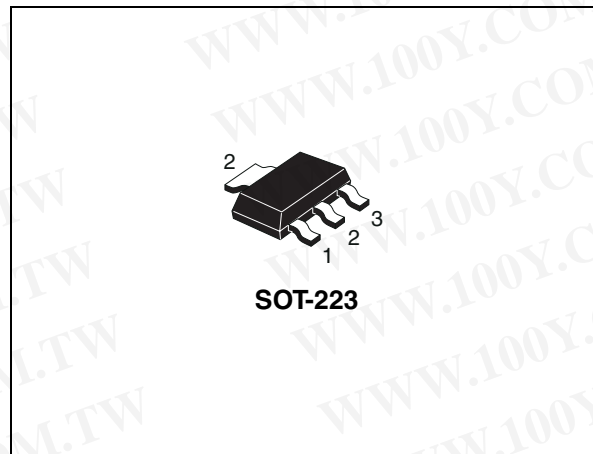
Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STN2NF10	100V	< 0.26Ω	2.4A

### Description

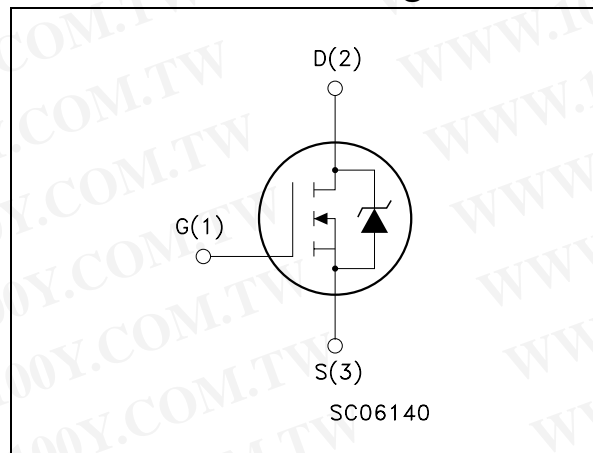
This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### Application

- Switching application
  - DC-DC converters



### Internal schematic diagram



### Order code

Part number	Marking	Package	Packaging
STN2NF10	N2NF10	SOT-223	Tape & reel

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS}=0$ )	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	2.4	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	1.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	17	A
	Derating factor	0.026	W/ $^\circ\text{C}$
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25^\circ\text{C}$	3.3	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	200	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	30	V/ns
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. This value is rated according to  $R_{thj-amb}$ ,  $t \leq 10\text{sec}$
3.  $I_{AS} = 2.4\text{A}$ ,  $V_{DD} = 30\text{V}$ ,  $R_g = 4.7\Omega$ , starting  $T_j = 25^\circ\text{C}$
4.  $I_{SD} \leq 6\text{A}$ ,  $di/dt \leq 500\text{A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	38	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(2)}$	Thermal resistance junction-amb	62.5	$^\circ\text{C}/\text{W}$

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz. Cu, ( $t < 10\text{sec}$ )
2. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz. Cu, ( $t > 10\text{sec}$ )

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## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating}, T_c = 125^{\circ}C$ $V_{DS} = 30V, T_c = 125^{\circ}C$			1 10 1	$\mu A$ $\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 1.2A$		0.23	0.26	$\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}$	Forward transconductance	$V_{DS} = 15V, I_D = 1.2A$		2.5		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1MHz, V_{GS} = 0$		280		pF
$C_{oss}$	Output capacitance			45		pF
$C_{rss}$	Reverse transfer capacitance			20		pF
$Q_g$	Total gate charge	$V_{DD} = 80V, I_D = 6A$		10	14	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10V$		2.5		nC
$Q_{gd}$	Gate-drain charge	(see Figure 15)		4		nC

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Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=50V$ , $I_D = 2.4A$ $V_{GS}=10V$ , $R_G=4.7\Omega$ (see Figure 14)		6 10		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=50V$ , $I_D = 2.4A$ $V_{GS}=10V$ , $R_G=4.7\Omega$ (see Figure 14)		20 3		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				2.4 17	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}= 2.4A$ , $V_{GS}=0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}= 6A$ , $V_{DD}=10V$ $di/dt=100A/\mu s$ , $T_j=150^\circ C$ (see Figure 19)		70 175 5		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 $\mu s$ , duty cycle 1.5%

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## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

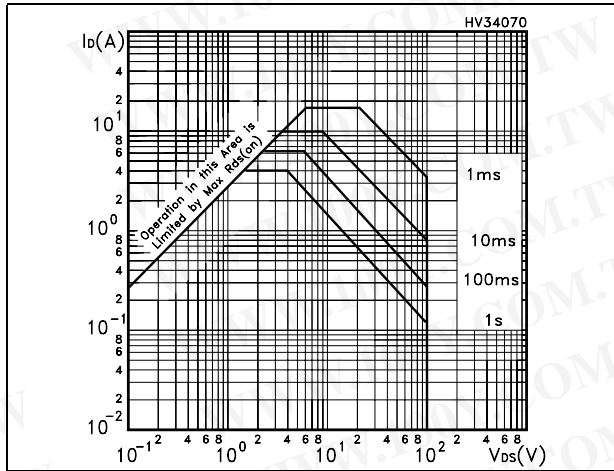


Figure 2. Thermal impedance

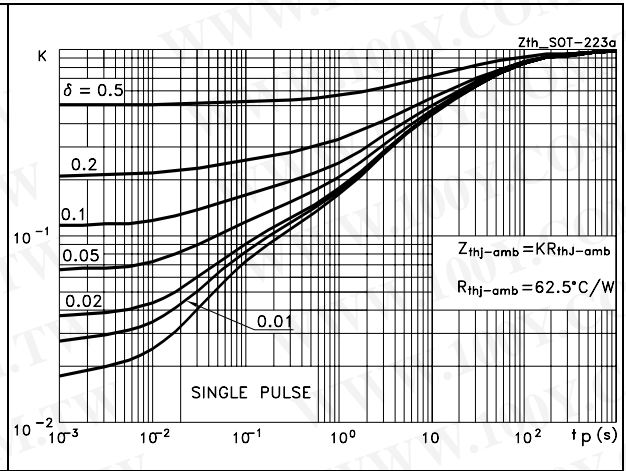


Figure 3. Output characteristics

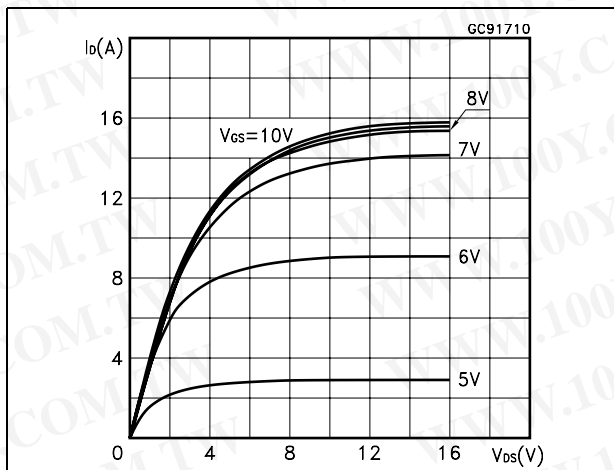


Figure 4. Transfer characteristics

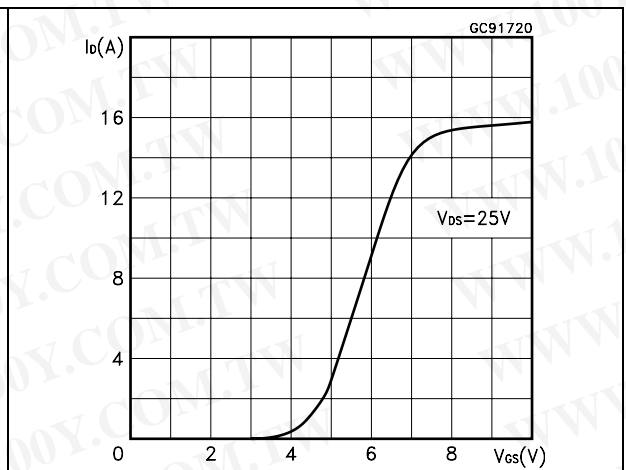


Figure 5. Transconductance

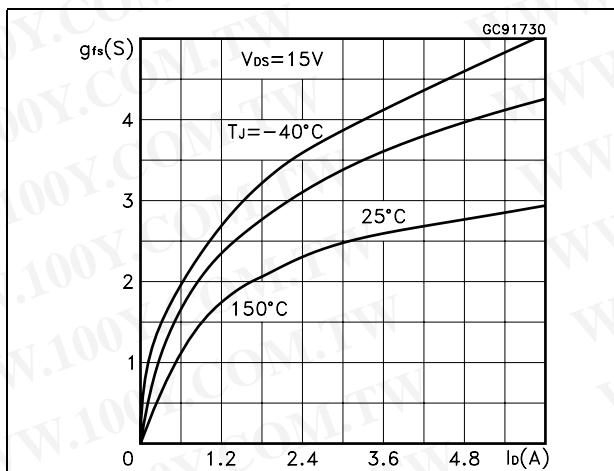
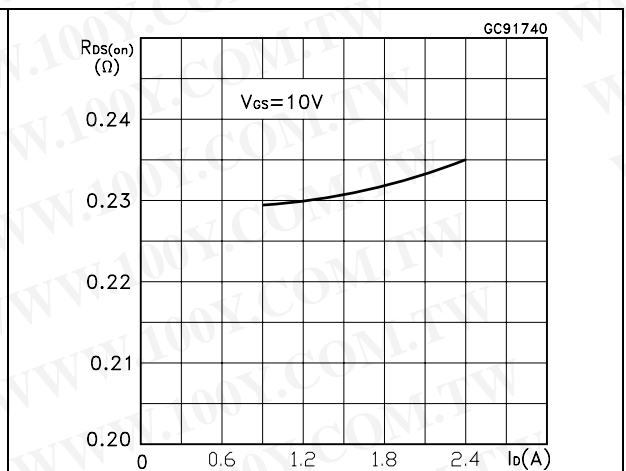
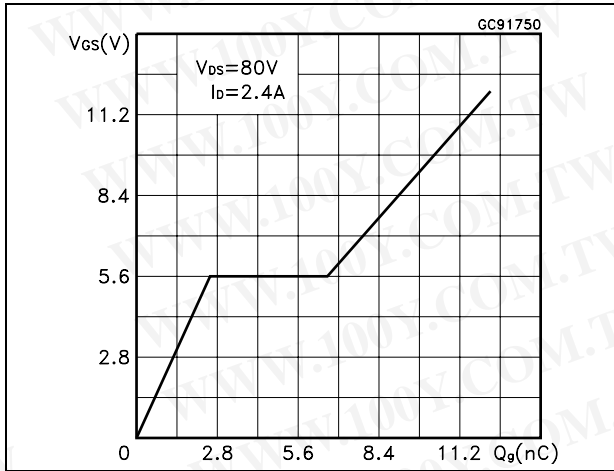


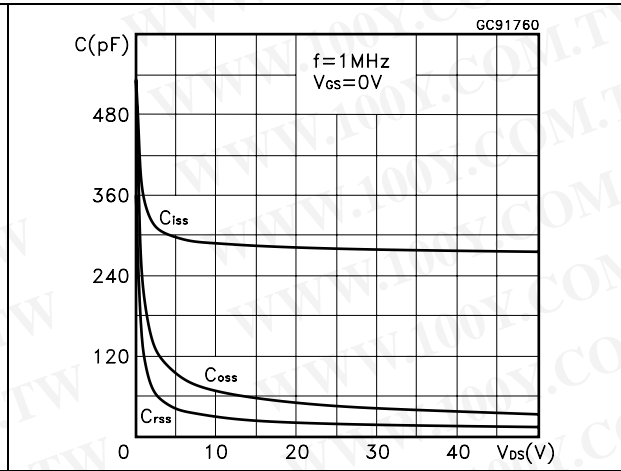
Figure 6. Static drain-source on resistance



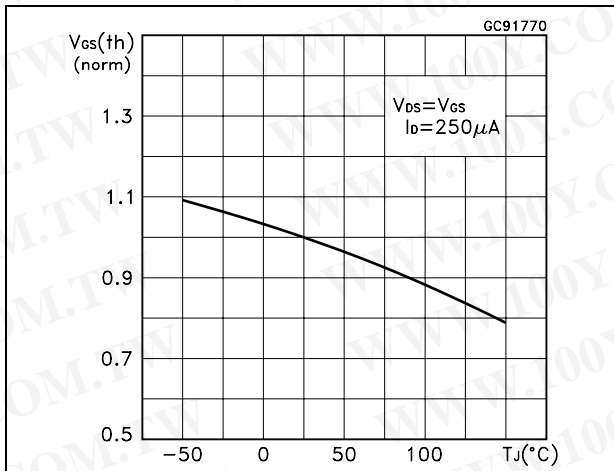
**Figure 7. Gate charge vs. gate-source voltage**



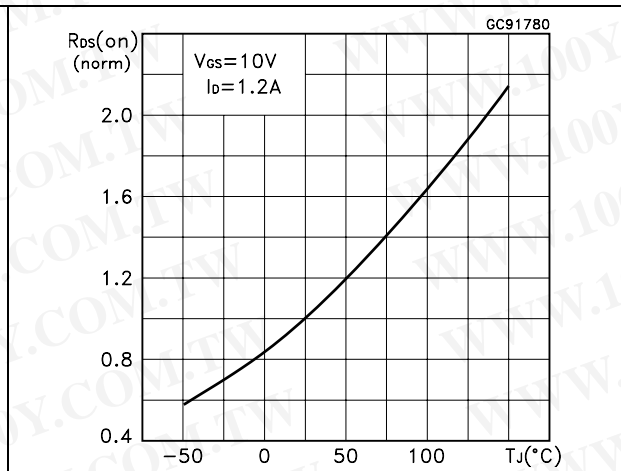
**Figure 8. Capacitance variations**



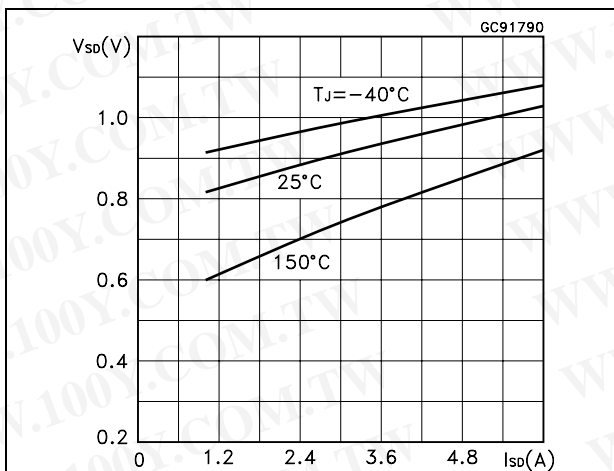
**Figure 9. Normalized gate threshold voltage vs. temperature**



**Figure 10. Normalized on resistance vs. temperature**



**Figure 11. Source-drain diode forward characteristics**



**Figure 12. Normalized BV<sub>DSS</sub> vs. temperature**

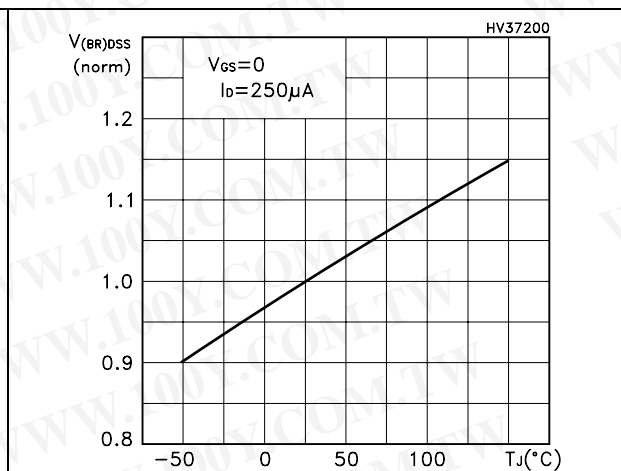
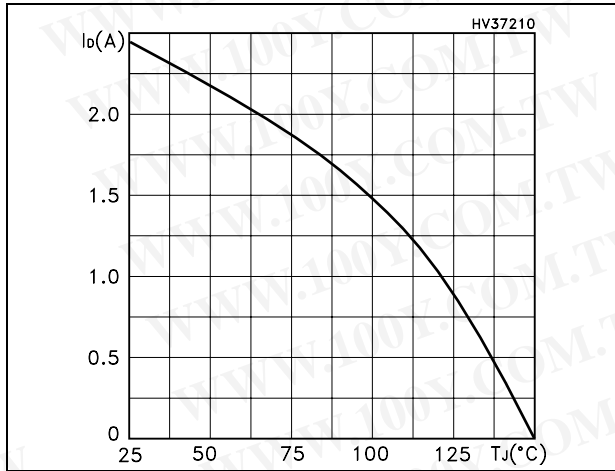


Figure 13. Max drain current vs. temperature



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### 3 Test circuit

Figure 14. Switching times test circuit for resistive load

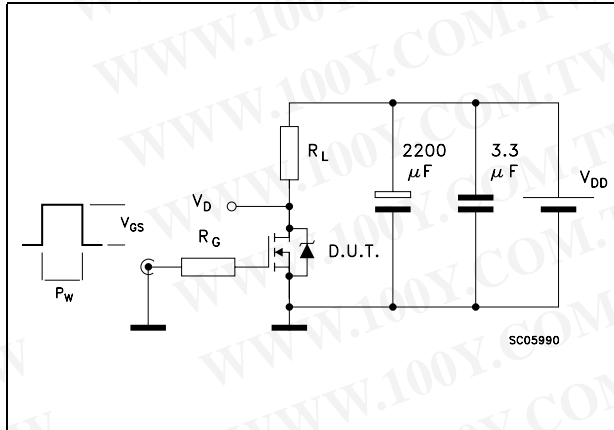


Figure 15. Gate charge test circuit

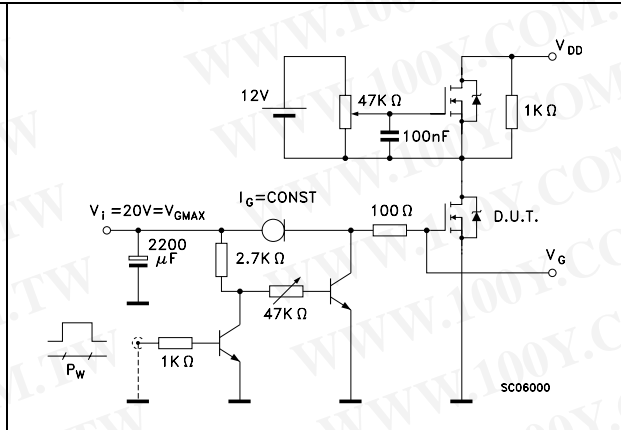


Figure 16. Test circuit for inductive load switching and diode recovery times

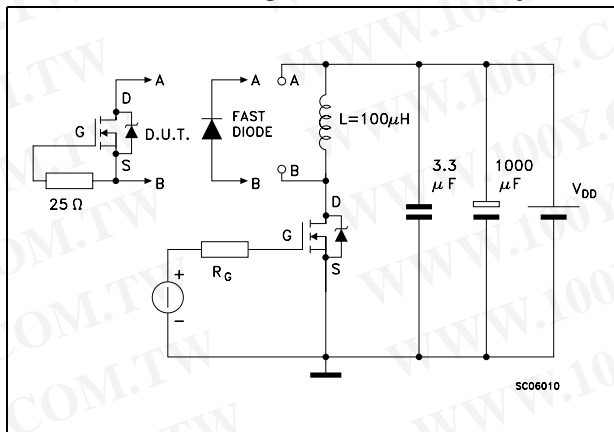


Figure 17. Unclamped inductive load test circuit

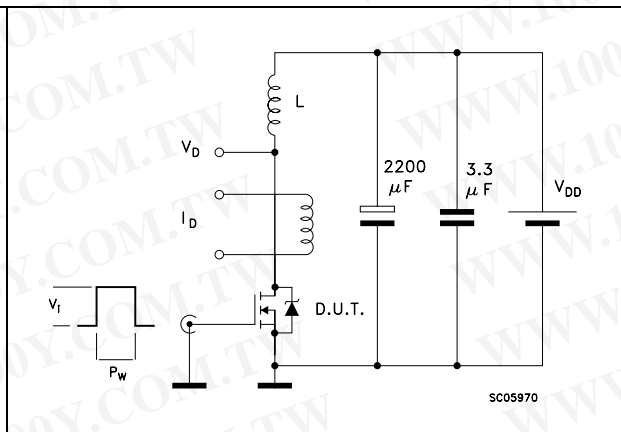


Figure 18. Unclamped inductive waveform

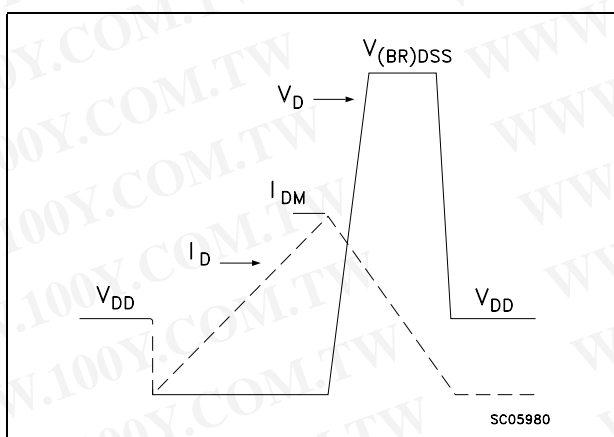
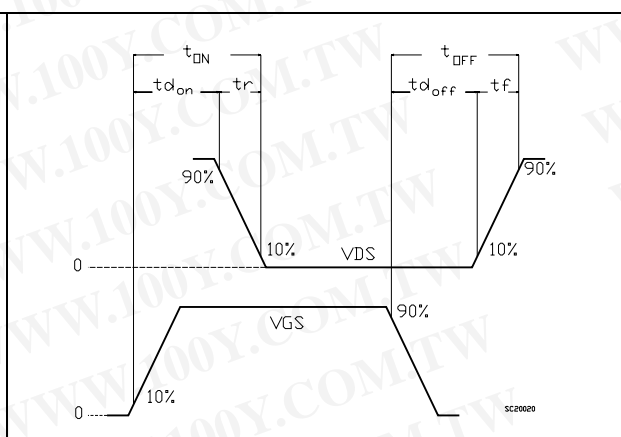


Figure 19. Switching time waveform

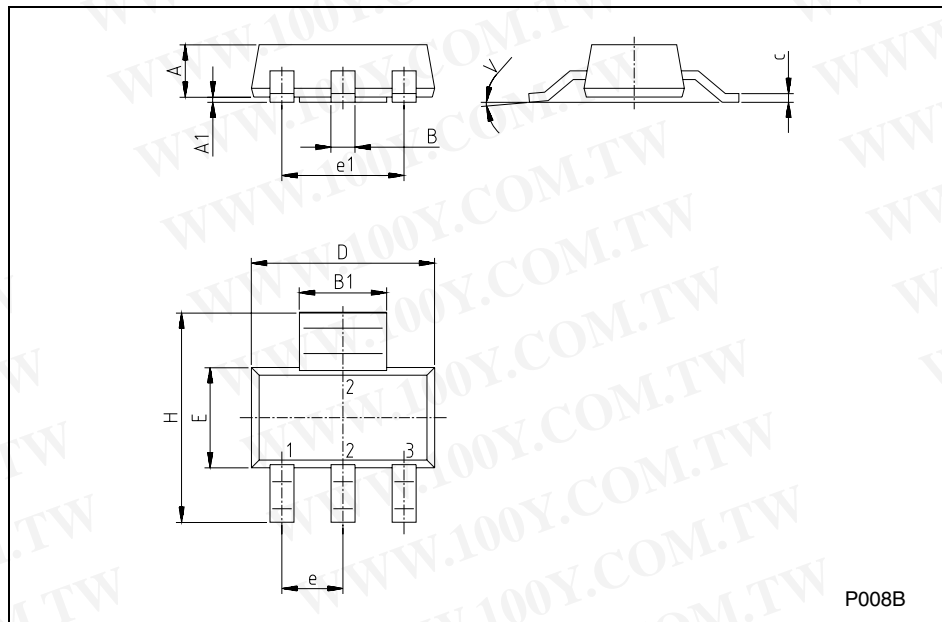


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

SOT-223 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10°			10°
A1		0.02				



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## 5 Revision history

Table 7. Revision history

Date	Revision	Changes
14-Sep-2006	4	The document has been reformatted
29-Mar-2007	5	<a href="#">Figure 1</a> has been updated
04-Apr-2007	6	New test condition for $I_{DSS}$ on <a href="#">Table 3</a>

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