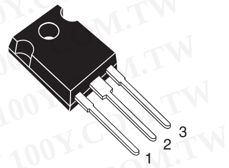
STGW40NC60KD

40 A - 600 V - short circuit rugged IGBT

Features

- Low on-voltage drop ($V_{CE(sat)}$)
- Low C_{res} / C_{ies} ratio (no cross conduction susceptibility)
- Short circuit withstand time 10 µs
- IGBT co-packaged with ultra fast free-wheeling diode



TO-247

Applications

- High frequency inverters
- Motor drivers

Description

This IGBT utilizes the advanced PowerMESH™ process resulting in an excellent trade-off between switching performance and low on-state behavior.

Figure 1. Internal schematic diagram

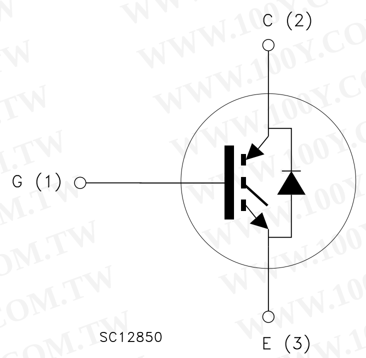


Table 1. Device summary

Order code	Marking	Package	Packaging
STGW40NC60KD	GW40NC60KD	TO-247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0)	600	V
I_C(1)	Collector current (continuous) at T_C = 25 °C	70	A
I_C(1)	Collector current (continuous) at T_C = 100 °C	38	A
I_{CL}(2)	Turn-off latching current	220	A
I_{CP}(3)	Pulsed collector current	220	A
V_{GE}	Gate-emitter voltage	±20	V
I_F	Diode RMS forward current at T_C = 25 °C	30	A
I_{FSM}	Surge non repetitive forward current t_p = 10 ms sinusoidal	120	A
P_{TOT}	Total dissipation at T_C = 25 °C	250	W
t_{scw}	Short circuit withstand time, V_{CE} = 0.5 $V_{(BR)CES}$ T_j = 125°C, R_G = 10 Ω, V_{GE} = 12 V	10	µs
T_j	Operating junction temperature	– 55 to 150	°C

1. Calculated according to the iterative formula:

$$I_c(T_c) = \frac{T_{J(MAX)} - T_c}{R_{thj-c} \times V_{CE(sat)(MAX)} \cdot (T_c, I_c)}$$

2. V_{clamp} = 80%,(V_{CES}), T_j =150°C, R_G = 10 Ω, V_{GE} = 15 V
3. Pulse width limited by max. junction temperature allowed

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case IGBT max.	0.5	°C/W
	Thermal resistance junction-case diode max.	1.5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage (V_{GE}= 0)	I_C= 1 mA	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE}= 15 V, I_C= 30 A V_{GE}= 15 V, I_C= 30 A, T_C= 125 °C		2.1 1.9	2.7	V V
I_{CES}	Collector cut-off current (V_{GE} = 0)	V_{CE} = 600 V V_{CE} = 600 V, T_C= 125 °C			500 5	µA mA
$V_{GE(th)}$	Gate threshold voltage	V_{CE}= V_{GE}, I_C= 250 µA	4.5		6.5	V
I_{GES}	Gate-emitter cut-off current (V_{CE} = 0)	V_{GE}= ±20 V			±100	nA
g_{fs} (1)	Forward transconductance	V_{CE} = 15 V , I_C = 30 A		20		S

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE}= 0		2870 295 69		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 480 V, I_C = 30 A, V_{GE} = 15 V *(see Figure 18)*		135 27 69.5		nC nC nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 480 V, I_C = 30 A R_G=10 Ω, V_{GE}= 15 V, *(see Figure 17)*		46 18.5 1530		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 480 V, I_C = 30 A R_G=10 Ω, V_{GE}= 15 V, T_C= 125 °C *(see Figure 17)*		45 19 1400		ns ns A/µs
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 480 V, I_C = 30 A R_G=10 Ω, V_{GE}= 15 V, *(see Figure 17)*		38 164 87		ns ns ns
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{cc} = 480 V, I_C = 30 A, R_G = 10 Ω, V_{GE} = 15 V T_C= 125 °C *(see Figure 17)*		70 208 130		ns ns ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
Eon E_{off} (1) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 480 V, I_C = 30 A R_G= 10 Ω, V_{GE}= 15 V, *(see Figure 17)*		595 716 311		µJ µJ µJ
Eon E_{off} (1) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 480 V, I_C = 30 A R_G= 10 Ω, V_{GE}= 15 V, T_C= 125 °C *(see Figure 17)*		808 1200 2008		µJ µJ µJ

1. Turn-off losses include also the tail of the collector current.

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on-voltage	I_F = 30 A I_F = 30 A, T_C = 125 °C		2.4 1.8		V V
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_F = 30 A,V_R = 50 V, di/dt = 100 A/µs *(see Figure 20)*		45 56 2.55		ns nC A
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_F = 30 A,V_R = 50 V, T_C =125 °C, di/dt = 100 A/µs *(see Figure 20)*		100 290 5.8		ns nC A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

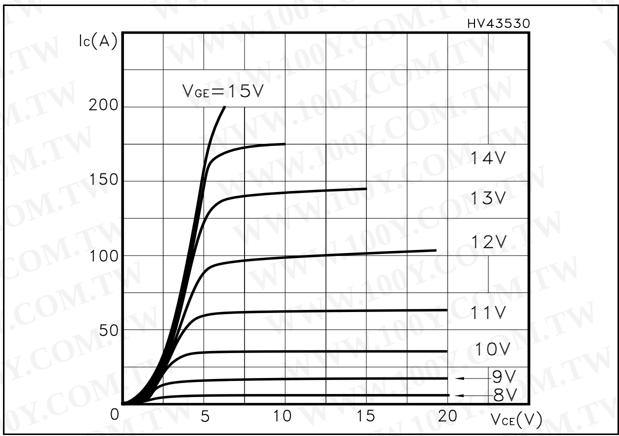


Figure 3. Transfer characteristics

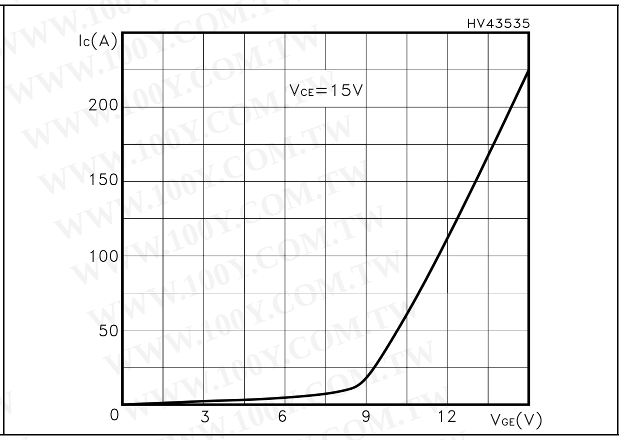


Figure 4. Transconductance

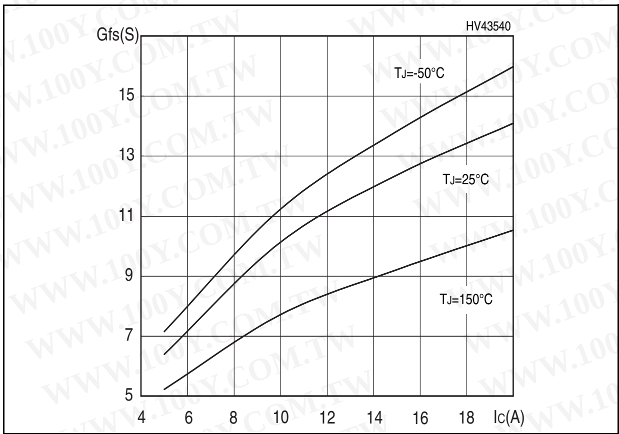


Figure 5. Collector-emitter on voltage vs temperature

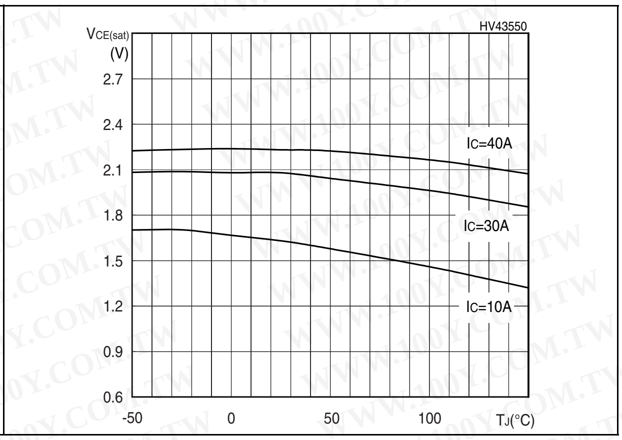


Figure 6. Gate charge vs gate-source voltage

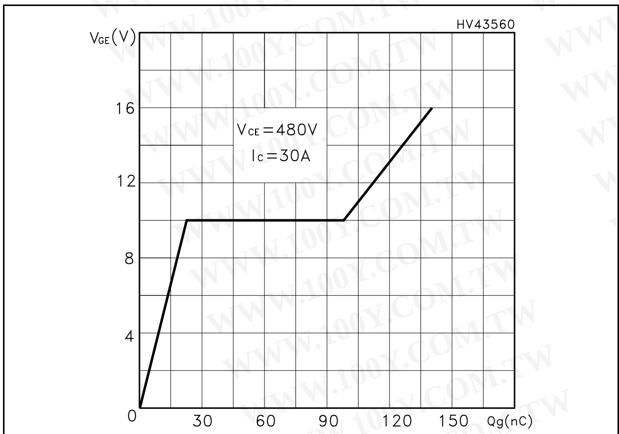


Figure 7. Capacitance variations

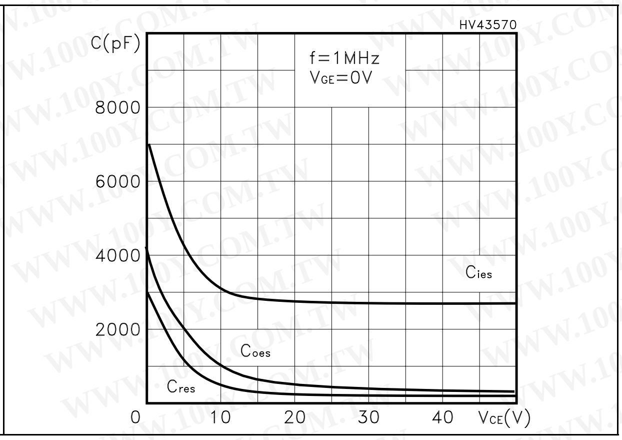


Figure 8. Normalized gate threshold voltage vs temperature

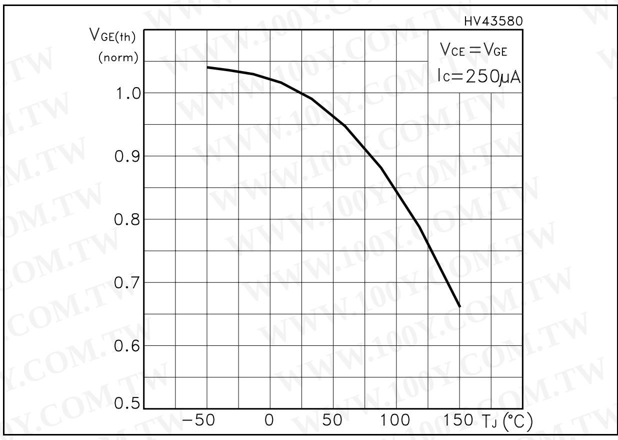


Figure 9. Collector-emitter on voltage vs collector current

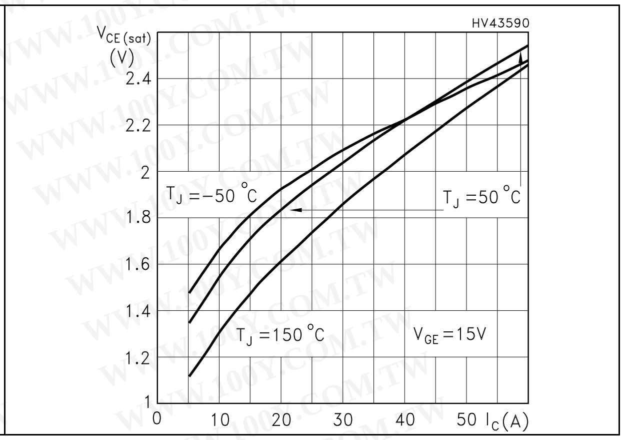


Figure 10. Normalized breakdown voltage vs temperature

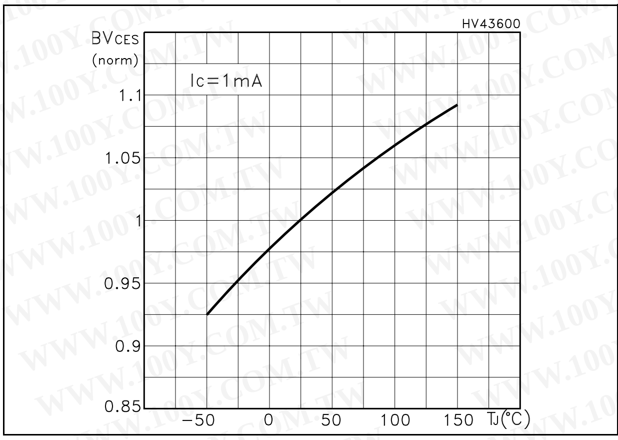


Figure 11. Switching losses vs temperature

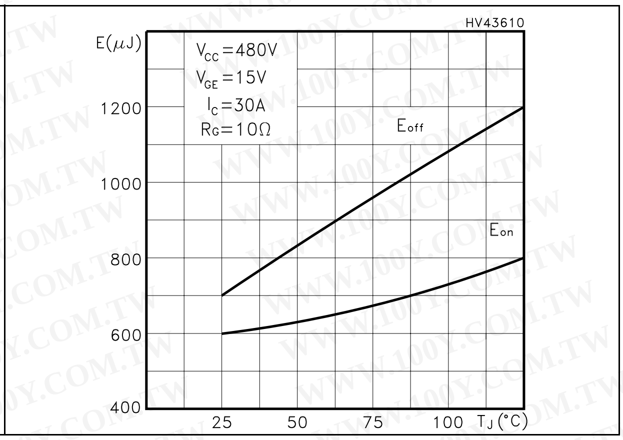


Figure 12. Switching losses vs gate resistance

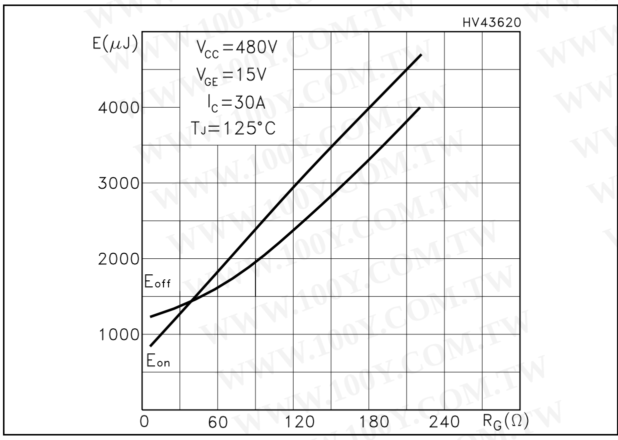


Figure 13. Switching losses vs collector current

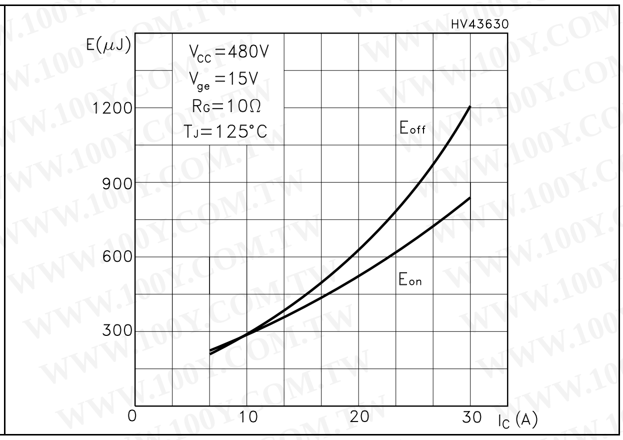


Figure 14. Thermal Impedance

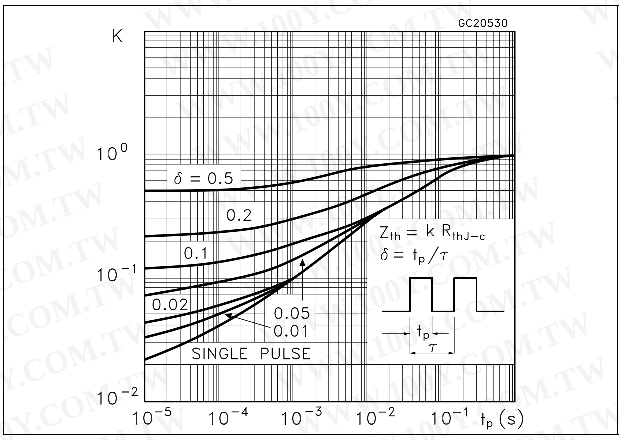


Figure 15. Turn-off SOA

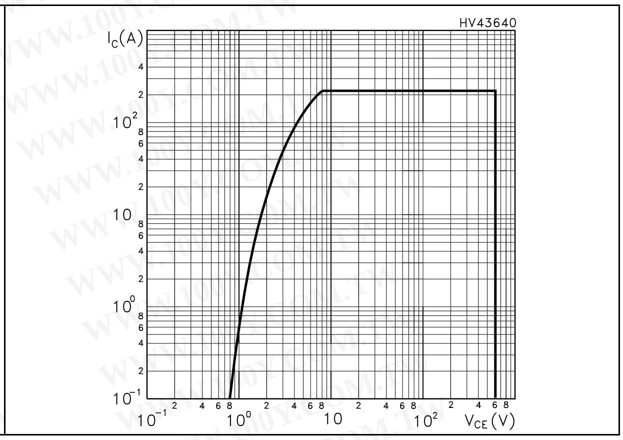
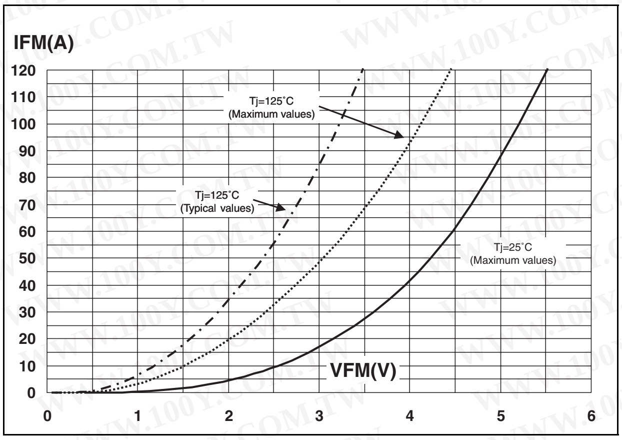


Figure 16. Forward voltage drop versus forward current



3 Test circuit

Figure 17. Test circuit for inductive load switching

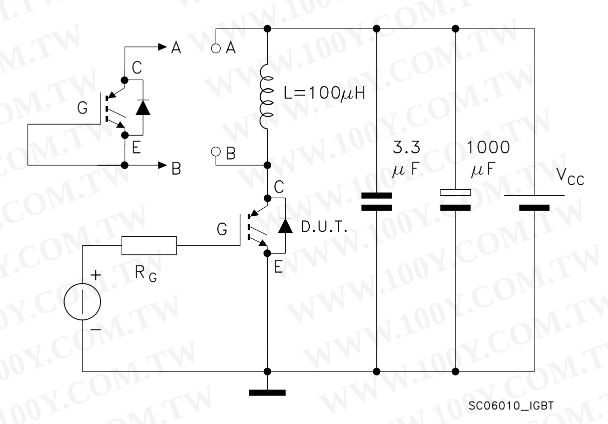


Figure 18. Gate charge test circuit

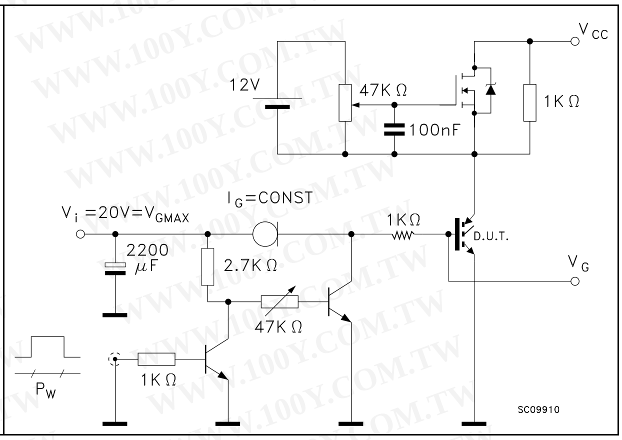


Figure 19. Switching waveforms

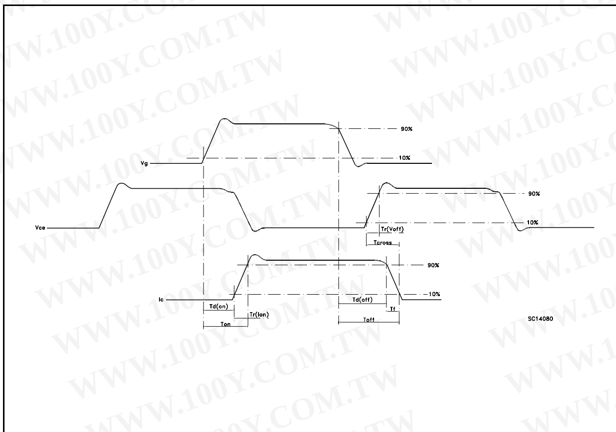
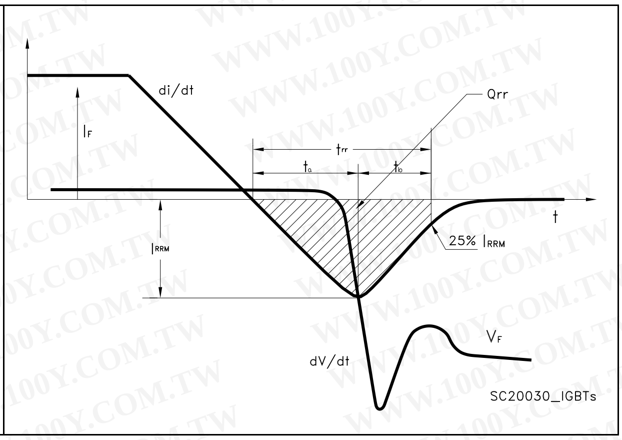


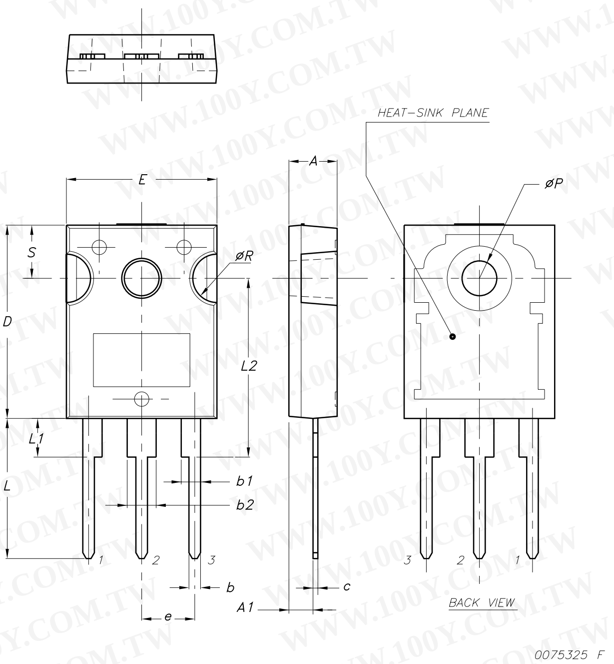
Figure 20. Diode recovery times waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-247 Mechanical data			
Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Jun-2008	1	Initial release