

Transistors

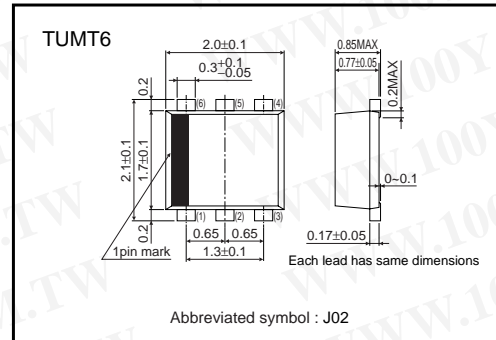
# Small switching (-20V, -1A)

## US6J2

●Features

- 1) Two Pch MOSFET transistors in a single TUMT6 package.
- 2) Mounting cost and area can be cut in half.
- 3) Low on-resistance.
- 4) Low voltage drive (2.5V) makes this device ideal for portable equipment.
- 5) Easily designed drive circuits.

●External dimensions (Unit : mm)



●Applications

switch

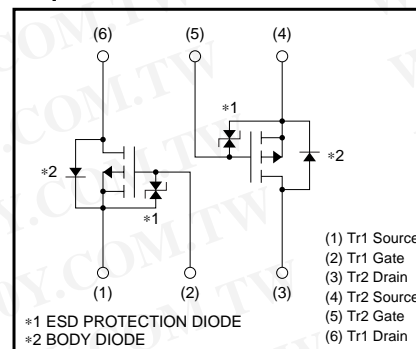
●Structure

Silicon P-channel  
 MOS FET

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US6J2		○

●Equivalent circuit



Transistors

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-source voltage	V <sub>DSS</sub>	-20	V
Gate-source voltage	V <sub>GSS</sub>	±12	V
Drain current	Continuous	I <sub>D</sub>	±1 A
	Pulsed	I <sub>DP</sub>	±4 A
Source current (Body diode)	Continuous	I <sub>S</sub>	-0.4 A
	Pulsed	I <sub>SP</sub>	-1.6 A
Total power dissipation	P <sub>D</sub>	1.0	W
Channel temperature	T <sub>ch</sub>	150	°C
Range of Storage temperature	T <sub>stg</sub>	-55 to +150	°C

\*1 P<sub>W</sub>≤10μs, Duty cycle≤50%  
 \*2 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	-	-	±10	μA	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	-20	-	-	V	I <sub>D</sub> =-1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	-	-	-1.0	μA	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	-0.7	-	-2.0	V	V <sub>DS</sub> =-10V, I <sub>D</sub> =-1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub>	-	280	390	mΩ	I <sub>D</sub> =-1A, V <sub>GS</sub> =-4.5V
		-	310	430	mΩ	I <sub>D</sub> =-1A, V <sub>GS</sub> =-4V
		-	570	800	mΩ	I <sub>D</sub> =-0.5A, V <sub>GS</sub> =-2.5V
Forward transfer admittance	Y <sub>fs</sub>	0.7	-	-	S	V <sub>DS</sub> =-10V, I <sub>D</sub> =-0.5A
Input capacitance	C <sub>iss</sub>	-	150	-	pF	V <sub>DS</sub> =-10V
Output capacitance	C <sub>oss</sub>	-	20	-	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	-	20	-	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub>	-	9	-	ns	I <sub>D</sub> =-0.5A
Rise time	t <sub>r</sub>	-	8	-	ns	V <sub>DD</sub> ≐-15V V <sub>GS</sub> =-4.5V
Turn-off delay time	t <sub>d(off)</sub>	-	5	-	ns	R <sub>L</sub> =30Ω
Fall time	t <sub>f</sub>	-	10	-	ns	R <sub>G</sub> =10Ω
Total gate charge	Q <sub>g</sub>	-	2.1	-	nC	V <sub>DD</sub> ≐-15V R <sub>L</sub> =15Ω
Gate-source charge	Q <sub>gs</sub>	-	0.5	-	nC	V <sub>GS</sub> =-4.5V R <sub>G</sub> =10Ω
Gate-drain charge	Q <sub>gd</sub>	-	0.5	-	nC	I <sub>D</sub> =-1A

**Transistors**

● **Electrical characteristic curves**

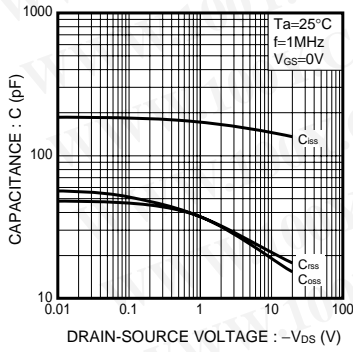


Fig.1 Typical Capacitance vs. Drain-Source Voltage

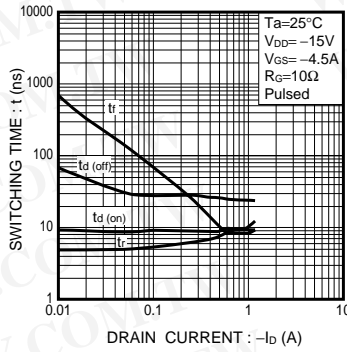


Fig.2 Switching Characteristics

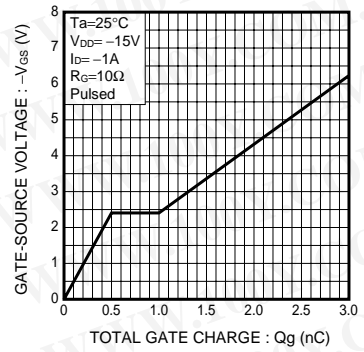


Fig.3 Dynamic Input Characteristics

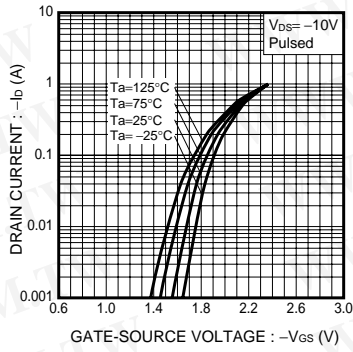


Fig.4 Typical Transfer Characteristics

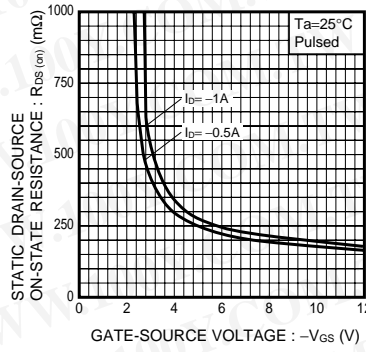


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

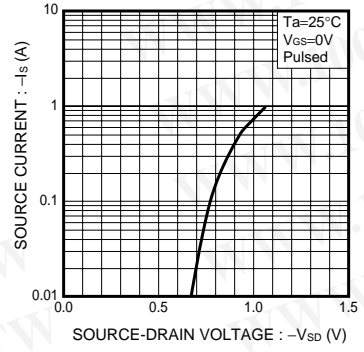


Fig.6 Source Current vs. Source-Drain Voltage

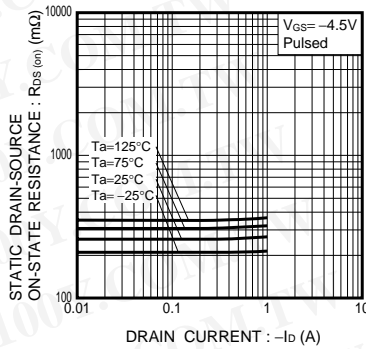


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (II)

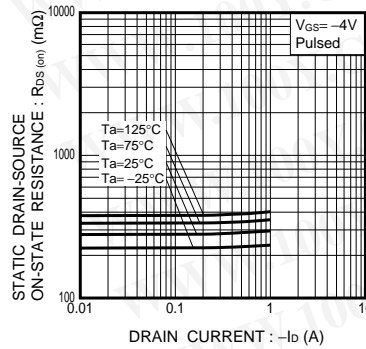


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (III)

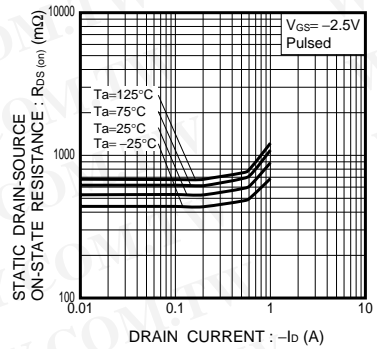


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (I)

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●Measurement circuits

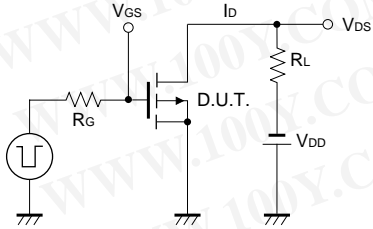


Fig.10 Switching Time Measurement Circuit

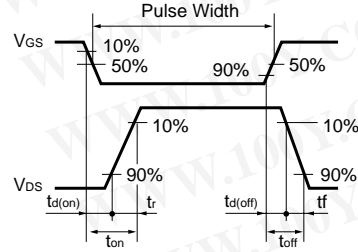


Fig.11 Switching Waveforms

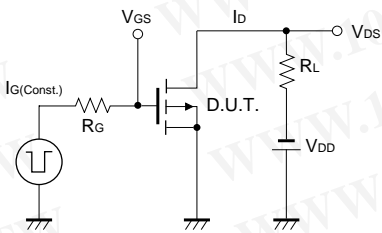


Fig.12 Gate Charge Measurement Circuit

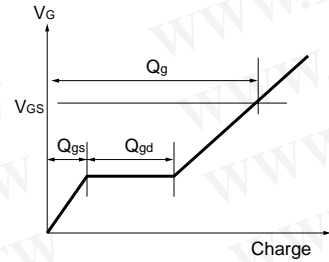


Fig.13 Gate Charge Waveform

## Appendix

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