

Transistor

2.5V Drive Pch+SBD MOS FET

QS5U28

●Structure

Silicon P-channel MOS FET
 Schottky Barrier DIODE

●Features

- 1) The QS5U28 combines Pch MOS FET with a Schottky barrier diode in TSMT5 package.
- 2) Low on-state resistance with fast switching.
- 3) Low voltage drive (2.5V).
- 4) Built-in schottky barrier diode has low forward voltage.

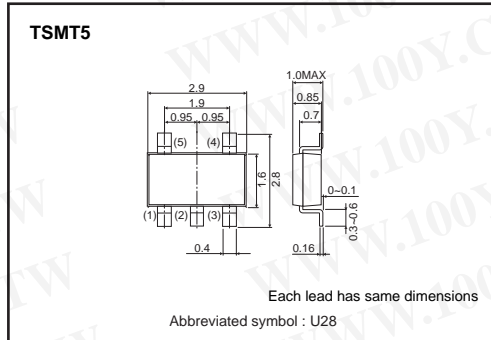
●Applications

Load switch, DC/DC conversion

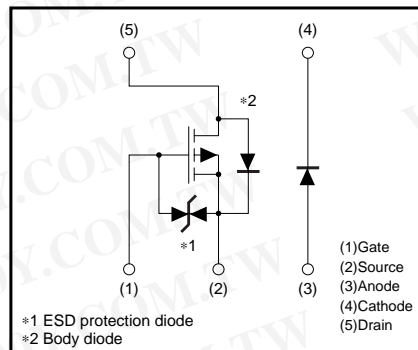
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS5U28		○

●External dimensions (Unit : mm)



●Equivalent circuit



* A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use. Use the protection circuit when rated voltages are exceeded.

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●Absolute maximum ratings (Ta=25°C)

<MOSFET>				
Parameter		Symbol	Limits	Unit
Drain-source voltage		V _{DSS}	-20	V
Gate-source voltage		V _{GSS}	±12	V
Drain current	Continuous	I _D	±2.0	A
	Pulsed	I _{DP} *1	±8.0	A
Source current (Body diode)	Continuous	I _S	-1.0	A
	Pulsed	I _{SP} *1	-8.0	A
Channel temperature		T _{ch}	150	°C
Power dissipation		P _D *3	0.9	W/ELEMENT

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Parameter		Symbol	Limits	Unit
Repetitive peak reverse voltage		V _{RM}	25	V
Reverse voltage		V _R	20	V
Forward current		I _F	1.0	A
Forward current surge peak		I _{FSM} *2	3.0	A
Junction temperature		T _j	150	°C
Power dissipation		P _D *3	0.7	W/ELEMENT

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Parameter		Symbol	Limits	Unit
Total power dissipation		P _D *3	1.25	W/TOTAL
Range of storage temperature		T _{stg}	-55 to +150	°C

*1 Pw≤10μs, Duty cycles≤1% *2 60Hz·1cyc. *3 Mounted on a ceramic board.

●Electrical characteristics (Ta=25°C)

<MOSFET>						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	-	-	±10	μA	V _{GS} = ±12V, V _{DS} = 0V
Drain-source breakdown voltage	V _{(BR)DSS}	-20	-	-	V	I _D = -1mA, V _{GS} = 0V
Zero gate voltage drain current	I _{BSS}	-	-	-1	μA	V _{DS} = -20V, V _{GS} = 0V
Gate threshold voltage	V _{GS(th)}	-0.7	-	-2.0	V	V _{DS} = -10V, I _D = -1mA
Static drain-source on-starte resistance	R _{DS(on)} *	-	90	125	mΩ	I _D = -2A, V _{GS} = -4.5V
		-	97	135	mΩ	I _D = -2A, V _{GS} = -4.0V
		-	175	245	mΩ	I _D = -1A, V _{GS} = -2.5V
Forward transfer admittance	Y _{fs} *	1.6	-	-	S	V _{DS} = -10V, I _D = -1A
Input capacitance	C _{iss}	-	450	-	pF	V _{DS} = -10V
Output capacitance	C _{oss}	-	70	-	pF	V _{GS} = 0V
Reverse transfer capacitance	C _{rss}	-	52	-	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	-	10	-	ns	V _{DD} = -15V V _{GS} = -4.5V
Rise time	t _r *	-	16	-	ns	I _D = -1A
Turn-off delay time	t _{d(off)} *	-	32	-	ns	R _L = 15Ω
Fall time	t _f *	-	15	-	ns	R _G = 10Ω
Total gate charge	Q _g *	-	4.8	-	nC	V _{DD} = -15V V _{GS} = -4.5V
Gate-source charge	Q _{gs} *	-	1.0	-	nC	I _D = -2A R _L = 7.5Ω
Gate-drain charge	Q _{gd} *	-	1.3	-	nC	R _G = 10Ω

* Pulsed

<MOSFET> Body diode (Source-drain)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD}	-	-	-1.2	V	I _S = -1.0V, V _{GS} = 0V

<Di>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _F	-	-	0.45	V	I _F = -1.0V
Reverse current	I _R	-	-	200	μA	V _R = 20V

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●Electrical characteristic curves

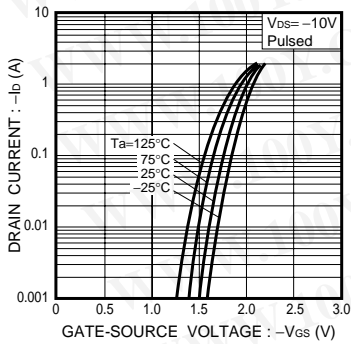


Fig.1 Typical Transfer Characteristics

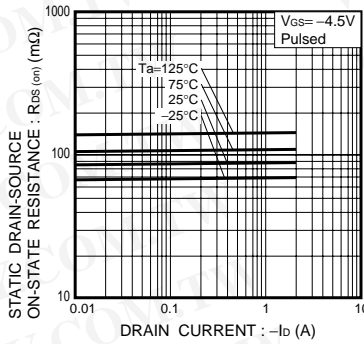


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current (I)

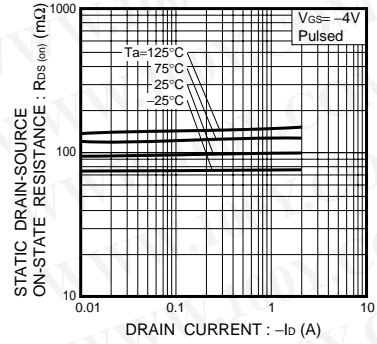


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (II)

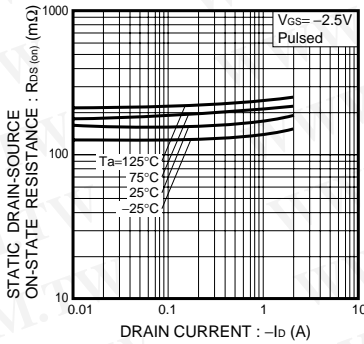


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (III)

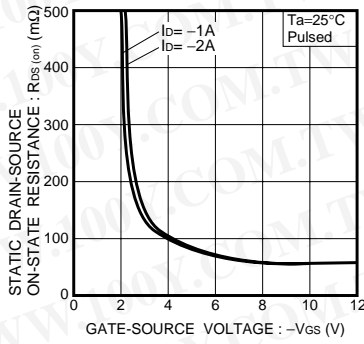


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

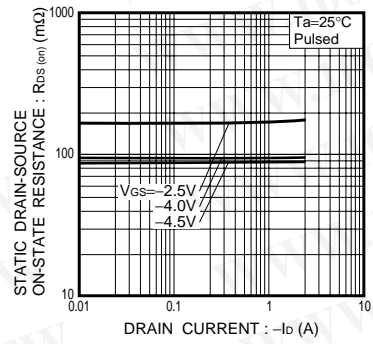


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

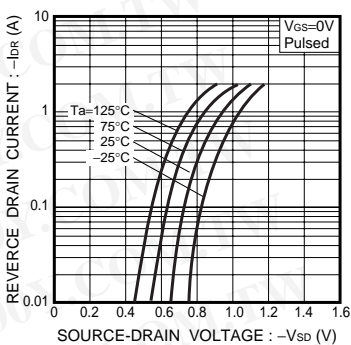


Fig.7 Reverse Drain Current vs. Source-Drain Voltage

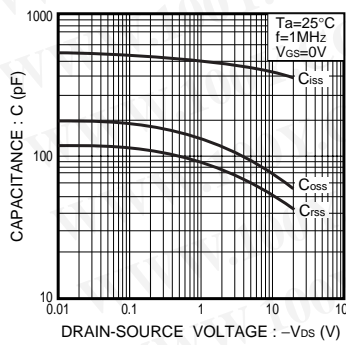


Fig.8 Typical Capacitance vs. Drain-Source Voltage

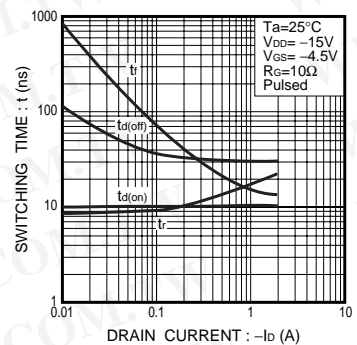


Fig.9 Switching Characteristics

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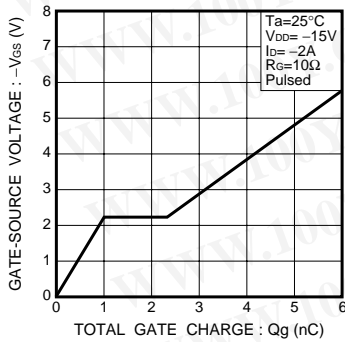


Fig.10 Dynamic Input Characteristics

● Measurement circuits

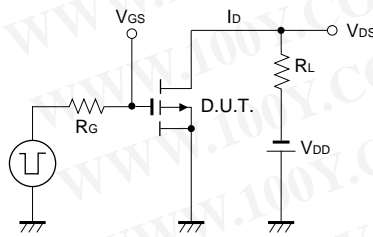


Fig.11 Switching Time Measurement Circuit

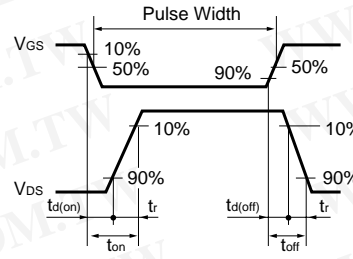


Fig.12 Switching Waveforms

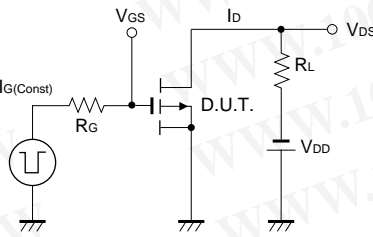


Fig.13 Gate Charge Measurement Circuit

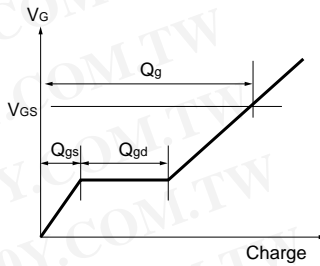


Fig.14 Gate Charge Waveforms

Appendix

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