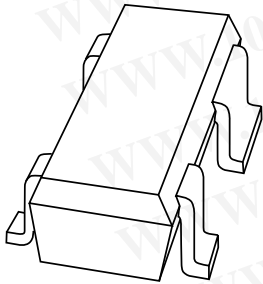


DATA SHEET



BFG480W NPN wideband transistor

Product specification
Supersedes data of 1998 Jul 09

1998 Oct 21

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NPN wideband transistor

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FEATURES

- High power gain
- High efficiency
- Low noise figure
- High transition frequency
- Emitter is thermal lead
- Low feedback capacitance
- Linear and non-linear operation.

APPLICATIONS

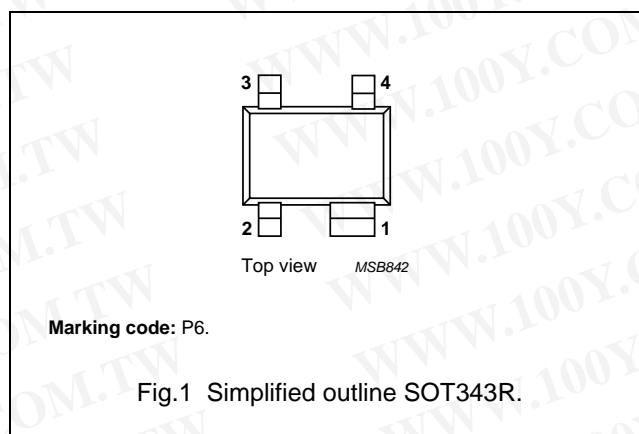
- RF front end with high linearity system demands (CDMA)
- Common emitter class AB driver.

DESCRIPTION

NPN double polysilicon wideband transistor with buried layer for low voltage applications in a 4-pin dual-emitter SOT343R plastic package.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	emitter
4	collector



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CE0}	collector-emitter voltage	open base	–	4.5	V
I_C	collector current (DC)		80	250	mA
P_{tot}	total power dissipation	$T_s \leq 60\text{ }^\circ\text{C}$	–	360	mW
f_T	transition frequency	$I_C = 80\text{ mA}; V_{CE} = 2\text{ V}; f = 2\text{ GHz}; T_{amb} = 25\text{ }^\circ\text{C}$	21	–	GHz
G_{max}	maximum gain	$I_C = 80\text{ mA}; V_{CE} = 2\text{ V}; f = 2\text{ GHz}; T_{amb} = 25\text{ }^\circ\text{C}$	16	–	dB
F	noise figure	$I_C = 8\text{ mA}; V_{CE} = 2\text{ V}; f = 2\text{ GHz}; \Gamma_S = \Gamma_{opt}$	1.8	–	dB
G_p	power gain	Pulsed; class-AB; $\delta < 1 : 2$; $t_p = 5\text{ ms}$; $V_{CE} = 3.6\text{ V}; f = 2\text{ GHz}; P_L = 100\text{ mW}$	13.5	–	dB
η_C	collector efficiency	Pulsed; class-AB; $\delta < 1 : 2$; $t_p = 5\text{ ms}$; $V_{CE} = 3.6\text{ V}; f = 2\text{ GHz}; P_L = 100\text{ mW}$	45	–	%

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	14.5	V
V _{CEO}	collector-emitter voltage	open base	–	4.5	V
V _{EBO}	emitter-base voltage	open collector	–	1	V
I _C	collector current (DC)		–	250	mA
P _{tot}	total power dissipation	T _s ≤ 60 °C; note 1; see Fig.2	–	360	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	150	°C

Note

1. T_s is the temperature at the soldering point of the emitter pins.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-s}	thermal resistance from junction to soldering point	250	K/W

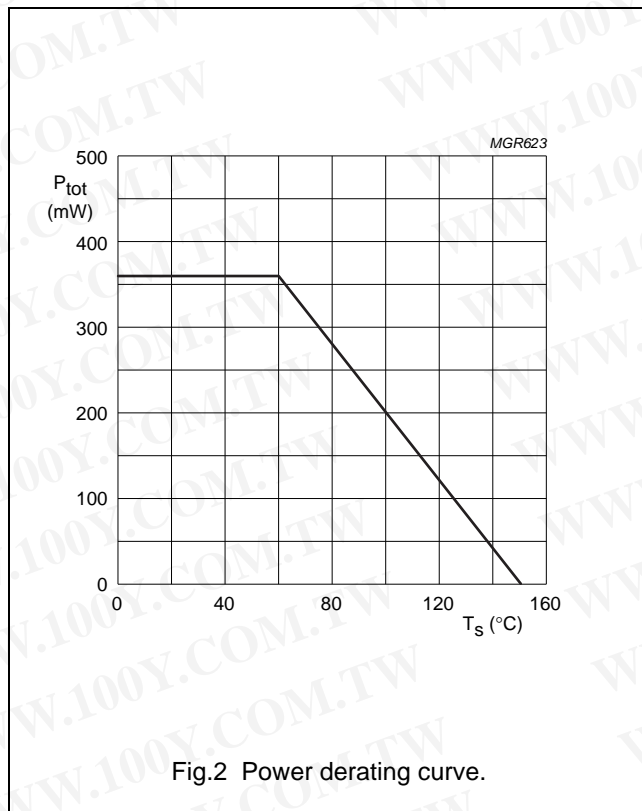


Fig.2 Power derating curve.

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CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 50\text{ }\mu\text{A}$; $I_E = 0$	14.5	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 5\text{ mA}$; $I_B = 0$	4.5	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	$I_E = 100\text{ }\mu\text{A}$; $I_C = 0$	1	–	–	V
I_{CBO}	collector-base leakage current	$V_{CE} = 5\text{ V}$; $V_{BE} = 0$	–	–	70	nA
h_{FE}	DC current gain	$I_C = 80\text{ mA}$; $V_{CE} = 2\text{ V}$; see Fig.3	40	60	100	
C_c	collector capacitance	$I_E = i_e = 0$; $V_{CB} = 2\text{ V}$; $f = 1\text{ MHz}$	–	1.4	–	pF
C_e	emitter capacitance	$I_C = i_c = 0$; $V_{EB} = 0.5\text{ V}$; $f = 1\text{ MHz}$	–	2.2	–	pF
C_{re}	feedback capacitance	$I_C = 0$; $V_{CB} = 2\text{ V}$; $f = 1\text{ MHz}$; see Fig.4	–	340	–	fF
f_T	transition frequency	$I_C = 80\text{ mA}$; $V_{CE} = 2\text{ V}$; $f = 2\text{ GHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; see Fig.5	–	21	–	GHz
G_{max}	maximum power gain; note 1	$I_C = 80\text{ mA}$; $V_{CE} = 2\text{ V}$; $f = 2\text{ GHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; see Figs 7 and 8	–	16	–	dB
$ S_{21} ^2$	insertion power gain	$I_C = 80\text{ mA}$; $V_{CE} = 2\text{ V}$; $f = 2\text{ GHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; see Fig.8	–	12	–	dB
F	noise figure	$I_C = 8\text{ mA}$; $V_{CE} = 2\text{ V}$; $f = 900\text{ MHz}$; $\Gamma_S = \Gamma_{opt}$; see Fig.13	–	1.2	–	dB
		$I_C = 8\text{ mA}$; $V_{CE} = 2\text{ V}$; $f = 2\text{ GHz}$; $\Gamma_S = \Gamma_{opt}$; see Fig.13	–	1.8	–	dB
PL_1	output power at 1 dB gain compression	Class-AB; $\delta < 1 : 2$; $t_p = 5\text{ ms}$; $V_{CE} = 3.6\text{ V}$; $I_{CQ} = 1\text{ mA}$; $f = 2\text{ GHz}$	–	20	–	dBm
ITO	third order intercept point	$I_C = 80\text{ mA}$; $V_{CE} = 2\text{ V}$; $f = 2\text{ GHz}$; $Z_S = Z_{S\text{ opt}}$; $Z_L = Z_{L\text{ opt}}$; note 2	–	28	–	dBm

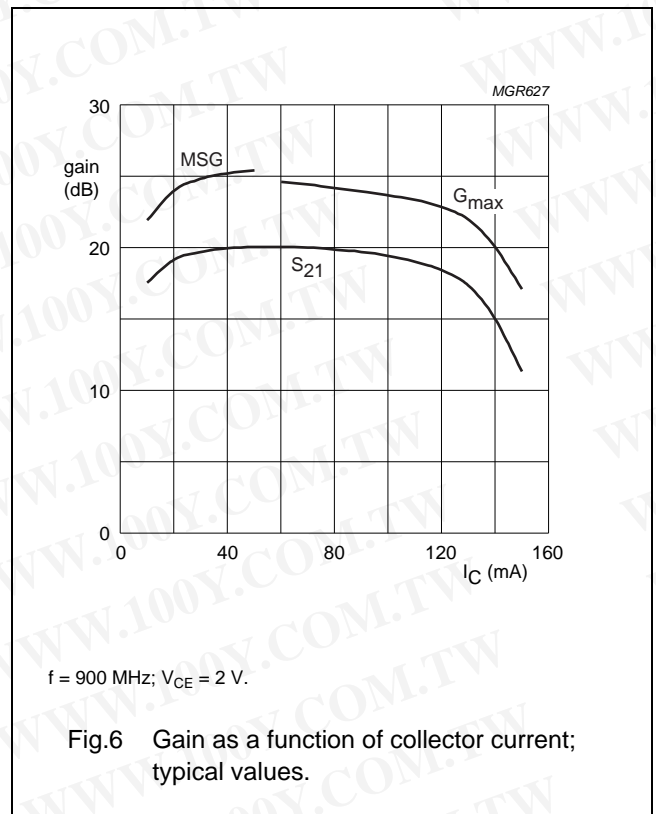
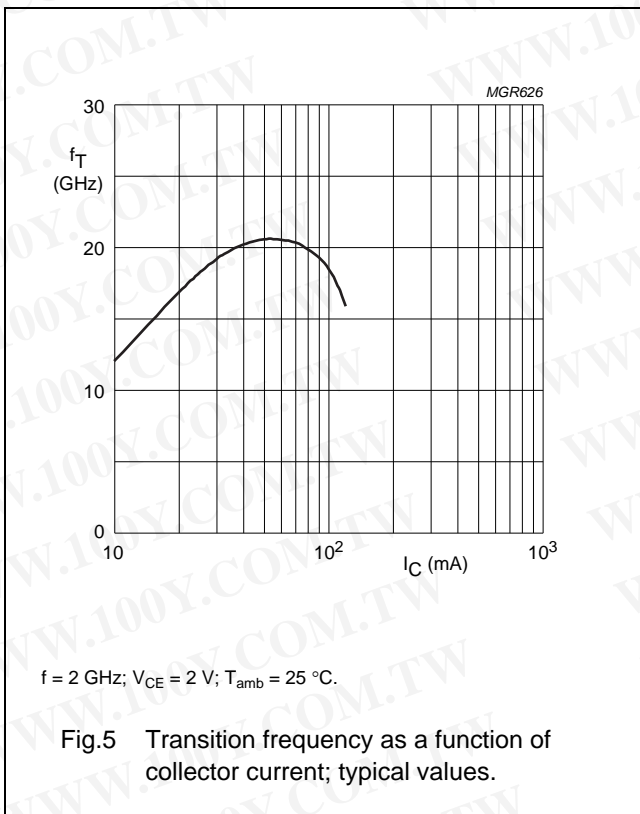
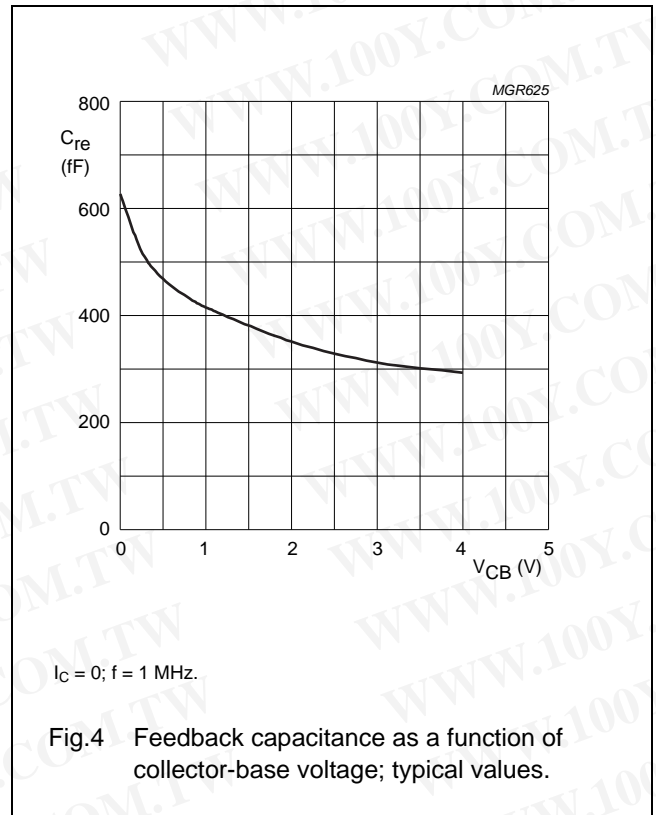
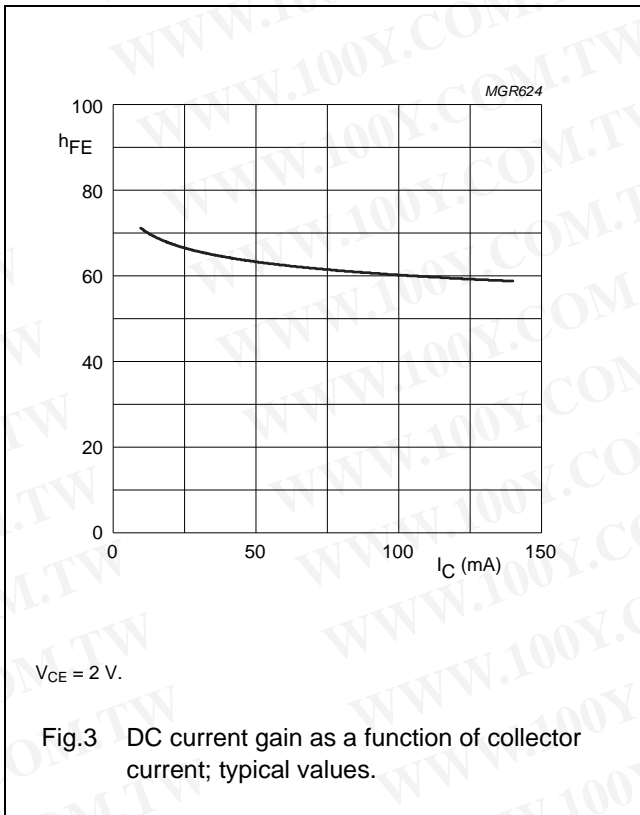
Notes

- G_{max} is the maximum power gain, if $K > 1$. If $K < 1$ then $G_{max} = \text{MSG}$; see Figs 6, 7 and 8.
- Z_S is optimized for noise; Z_L is optimized for gain.

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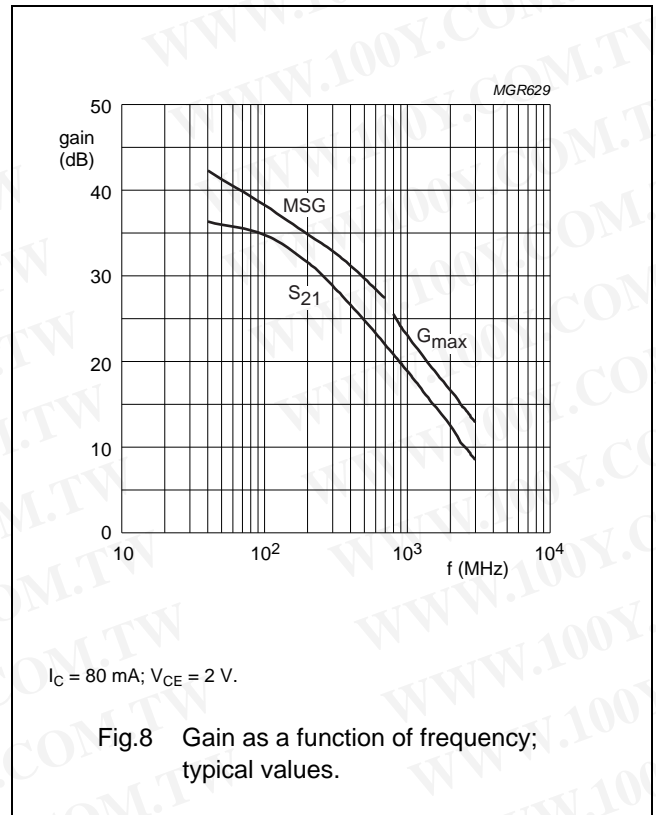
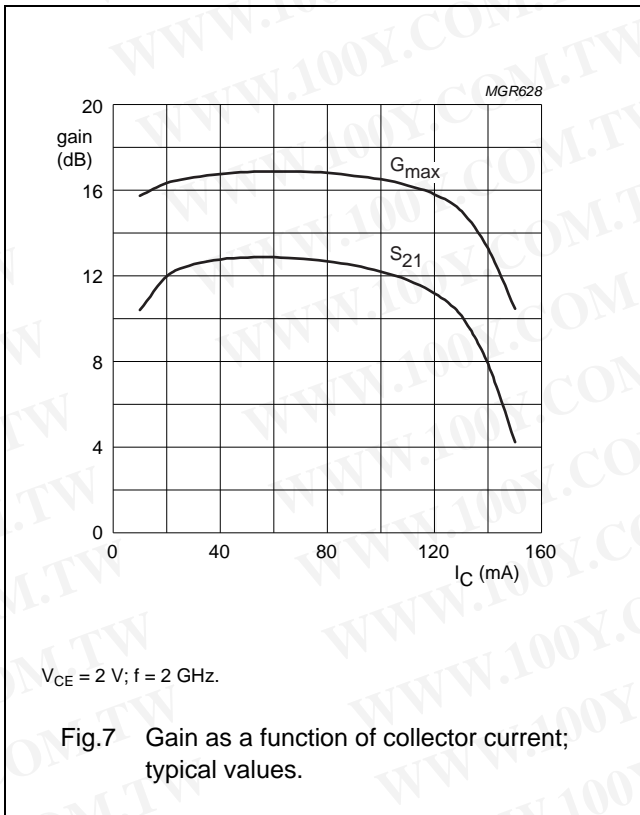
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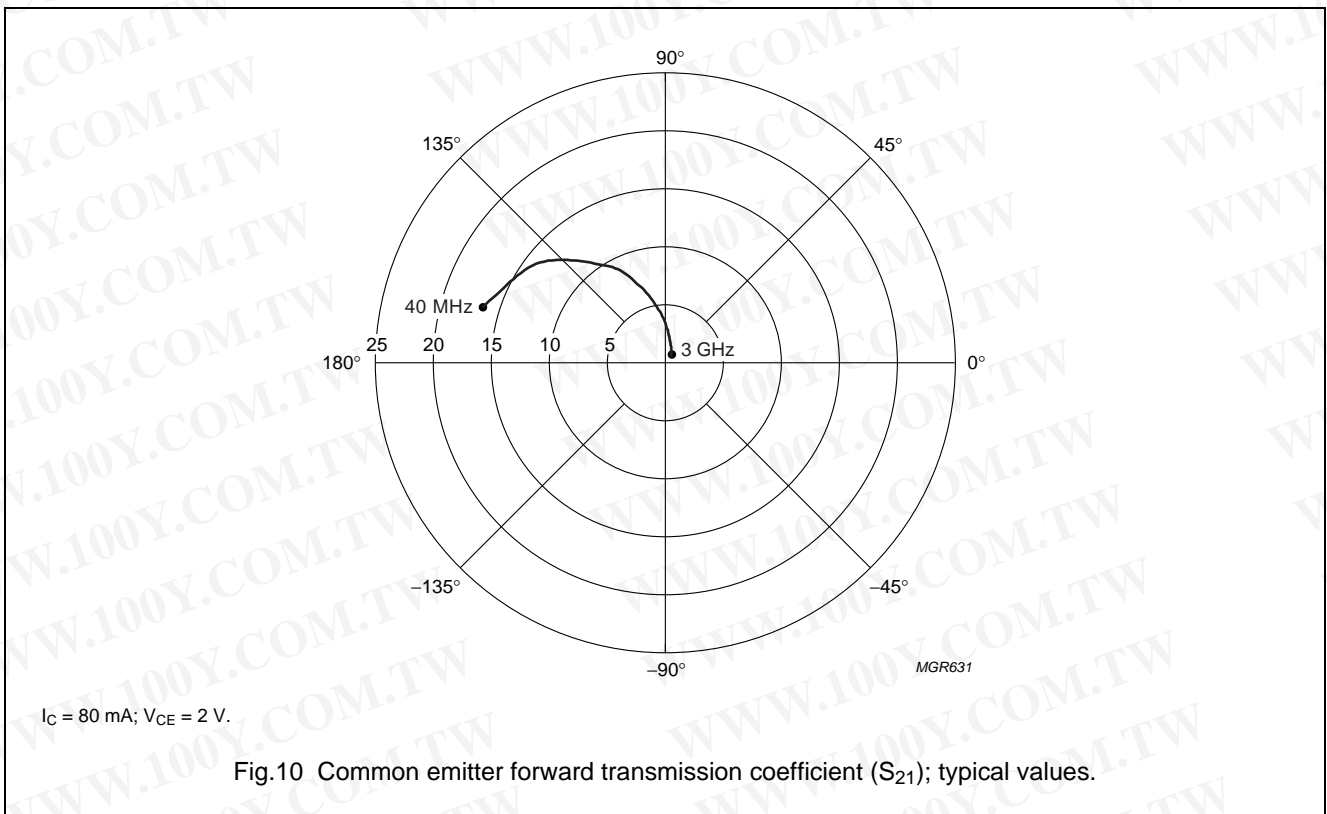
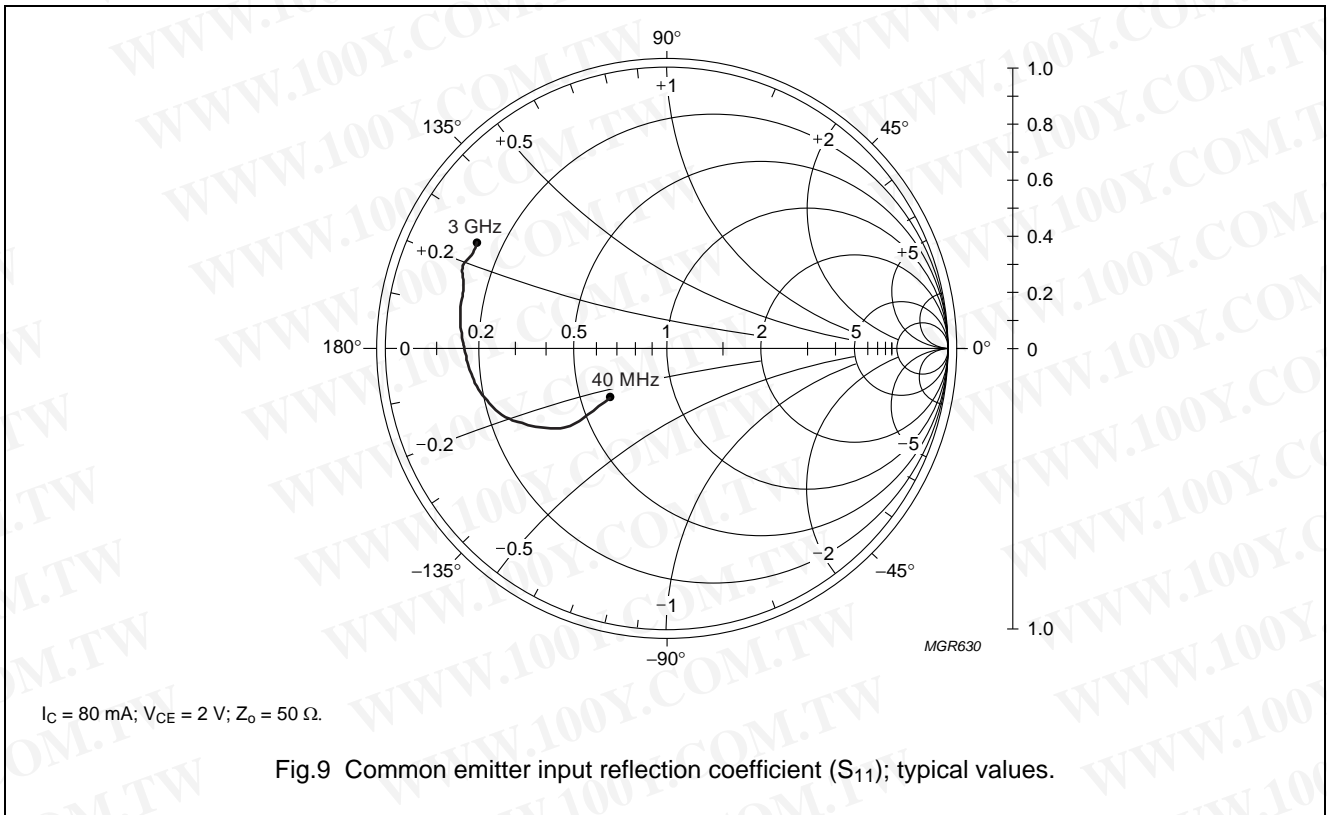
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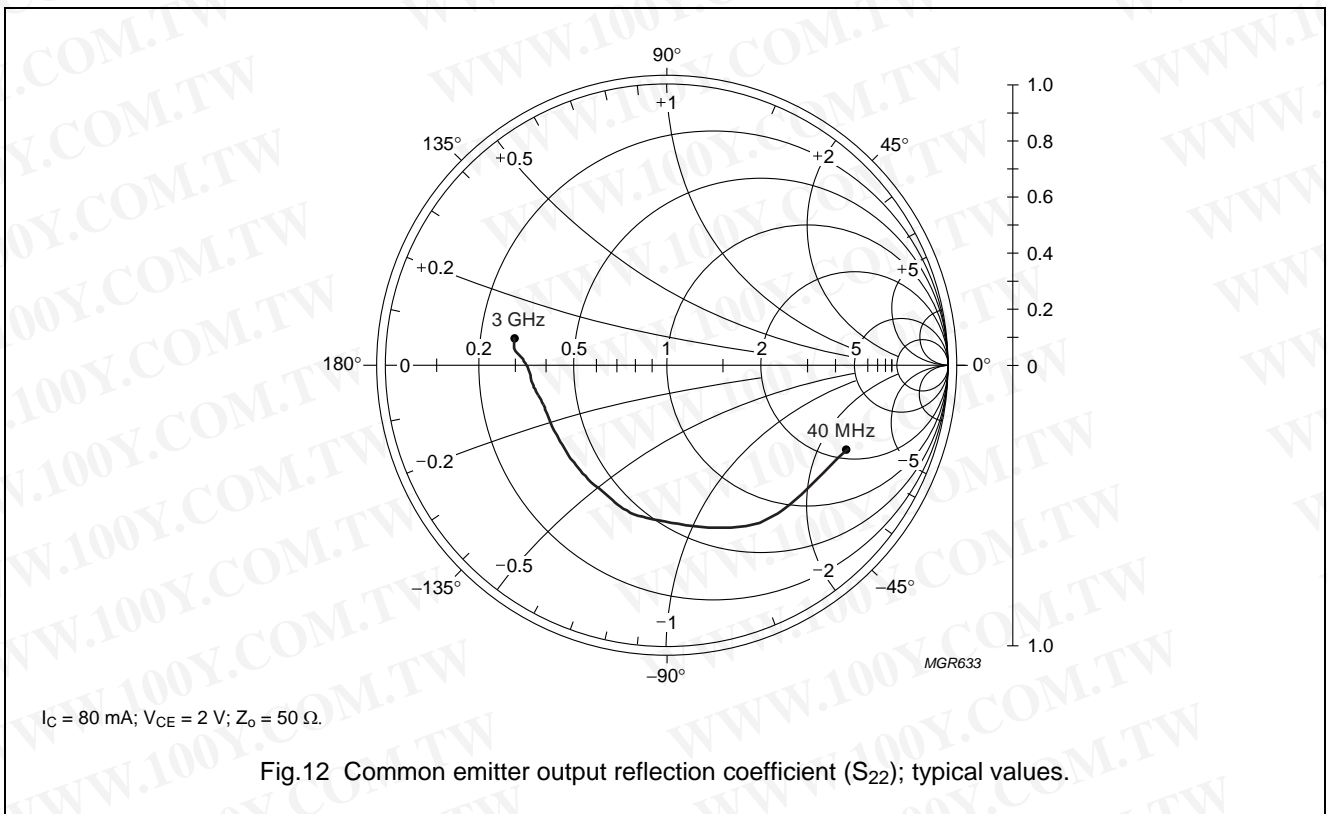
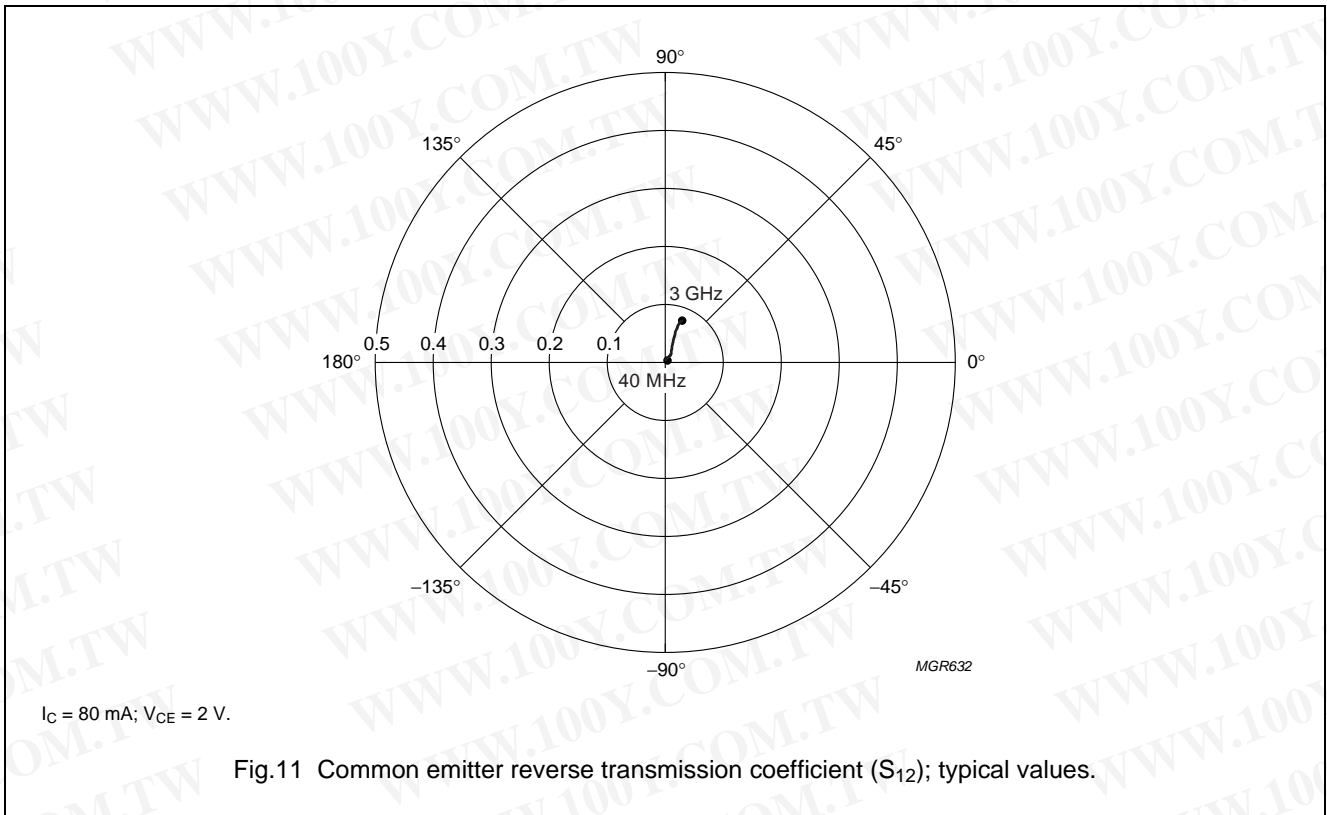
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Noise data

$V_{CE} = 2\text{ V}$; typical values.

f (MHz)	I _C (mA)	F _{min} (dB)	Γ _{mag}	Γ _{angle}	r _n (Ω)
900	2	1.1	0.41	96.1	0.21
	4	1.1	0.31	106.6	0.14
	6	1.2	0.27	118.4	0.12
	8	1.2	0.26	131.7	0.10
	10	1.3	0.28	143.2	0.10
	20	1.6	0.39	166.2	0.07
	40	2.0	0.49	176.0	0.07
	60	2.3	0.57	179.5	0.07
2000	80	2.9	0.45	177.3	0.18
	2	2.4	0.57	171.9	0.09
	4	2.0	0.49	178.9	0.08
	6	1.8	0.46	-175.7	0.09
	8	1.8	0.44	-171.7	0.09
	10	1.8	0.43	-168.4	0.09
	12	1.8	0.44	-165.3	0.10
	14	1.8	0.44	-163.7	0.10
	20	1.9	0.46	-158.3	0.11
	40	2.3	0.52	-150.2	0.14
	60	2.6	0.56	-147.7	0.18
	80	2.8	0.60	-146.1	0.22

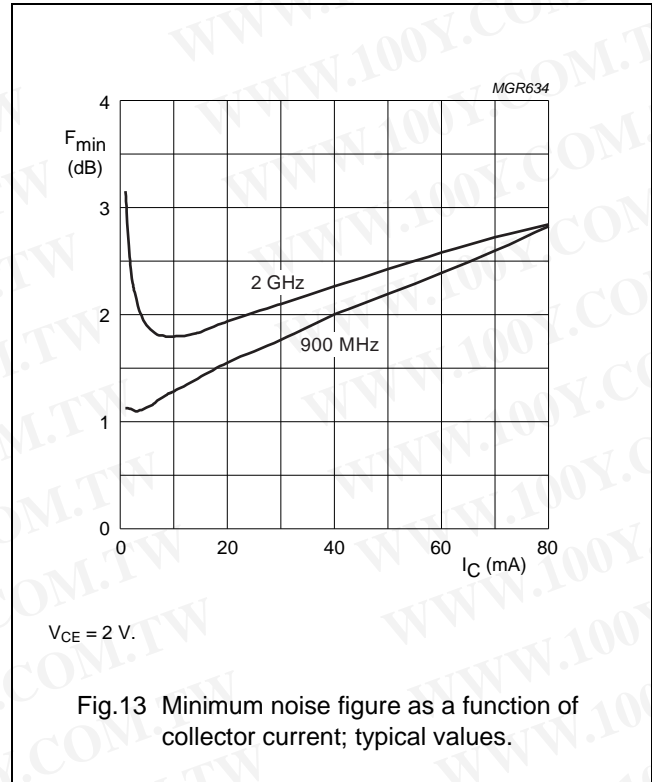


Fig.13 Minimum noise figure as a function of collector current; typical values.

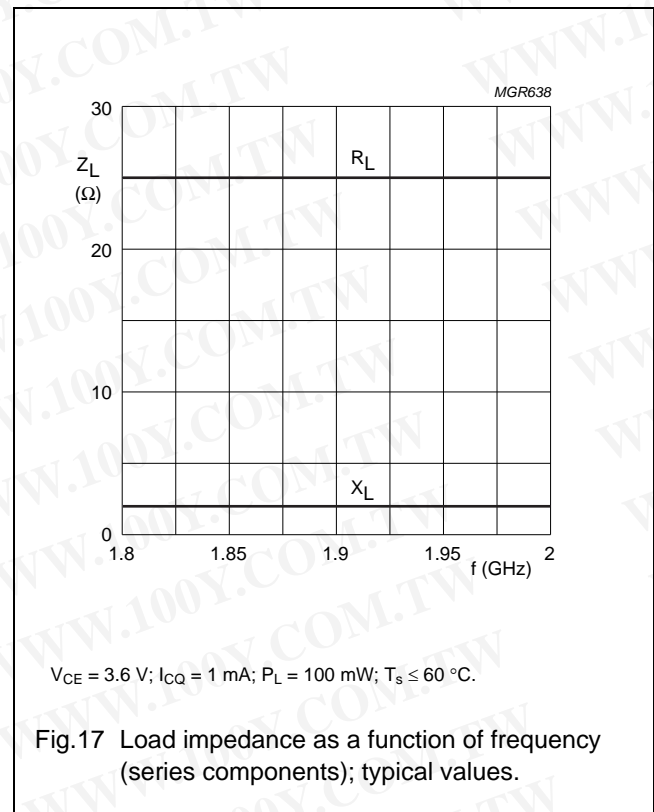
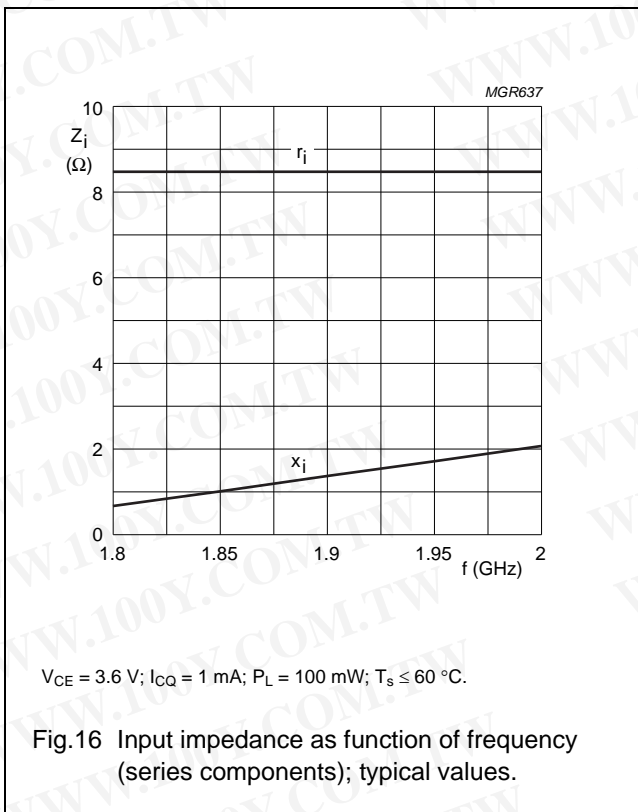
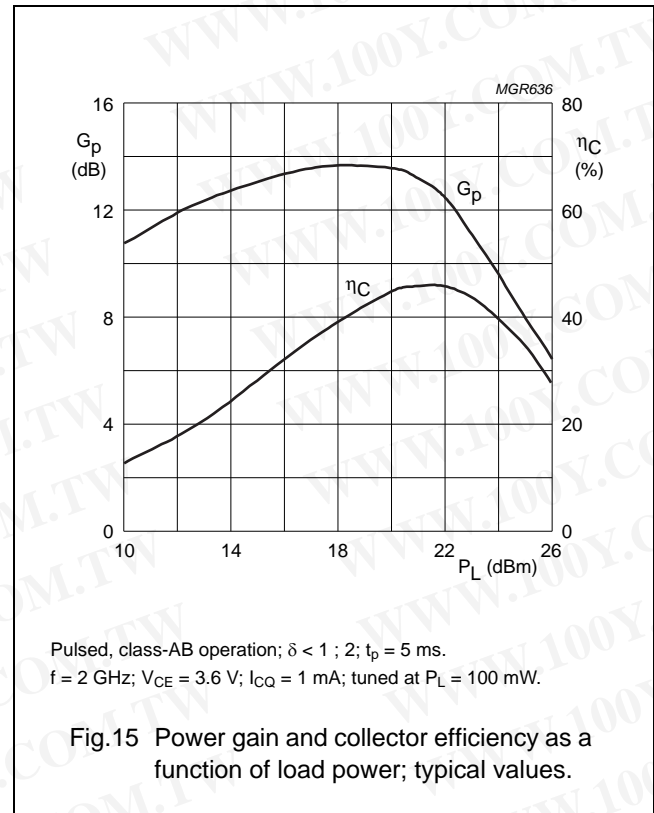
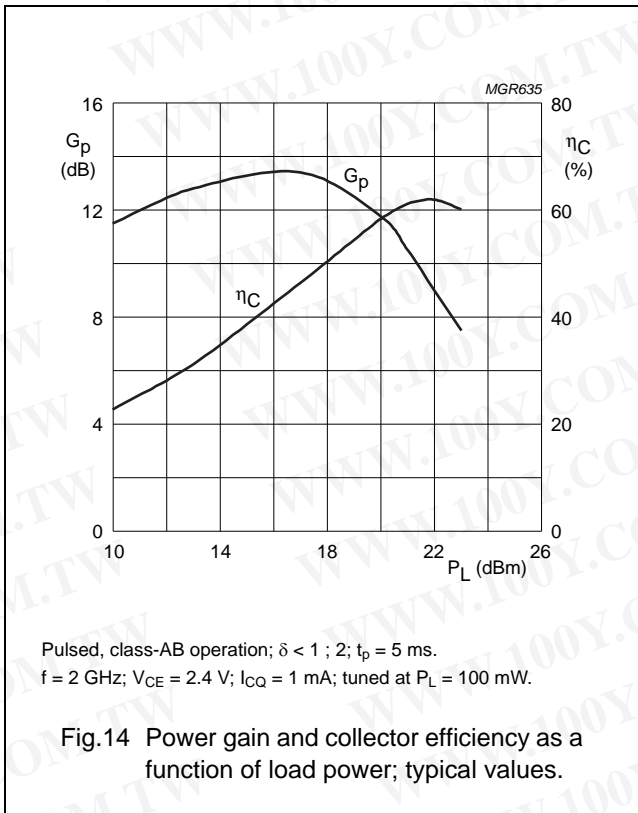
APPLICATION INFORMATION

RF performance at $T_s \leq 60\text{ °C}$ in a common emitter test circuit (see Figs 18 and 19).

MODE OF OPERATION	f (GHz)	V _{CE} (V)	I _{CQ} (mA)	P _L (mW)	G _p (dB)	η _c (%)
Pulsed; class-AB; δ < 1 : 2; t _p = 5 ms	2	3.6	1	100	typ. 13.5	typ. 45

NPN wideband transistor

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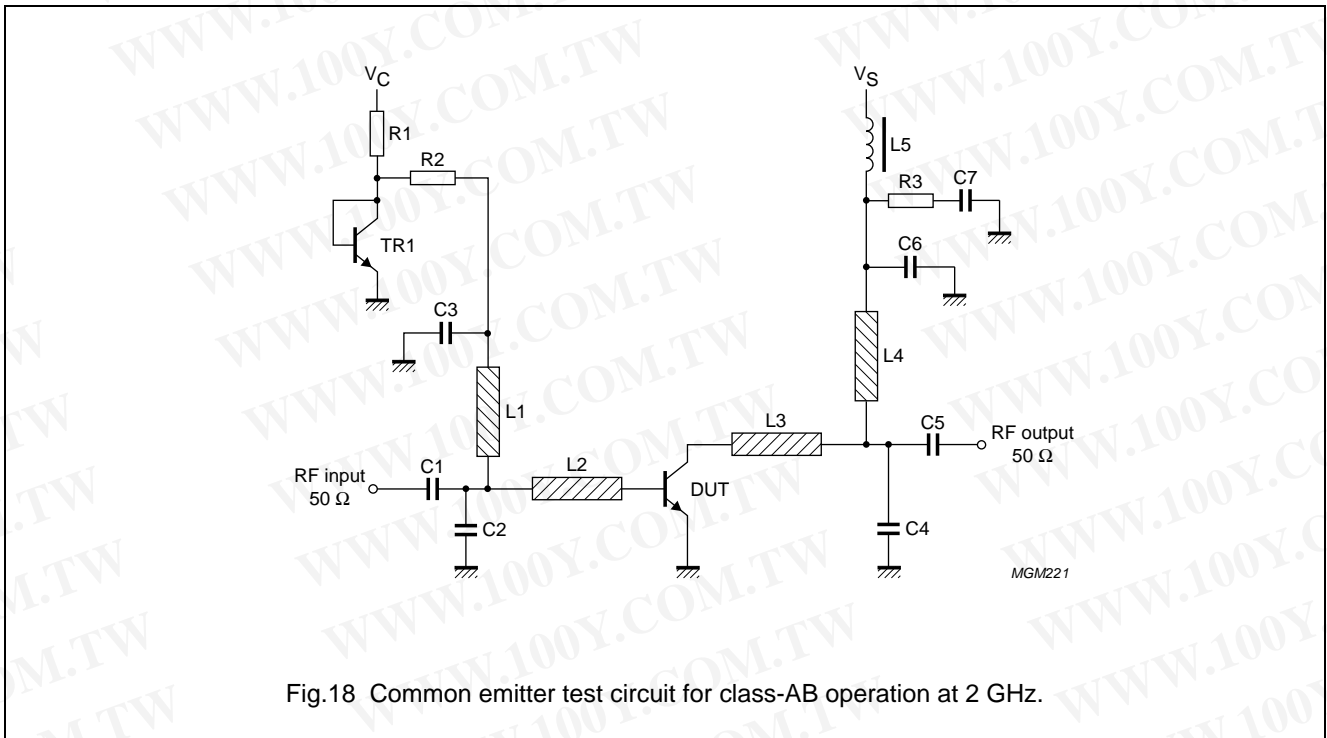


Fig.18 Common emitter test circuit for class-AB operation at 2 GHz.

List of components used in test circuit (see Figs 18 and 19)

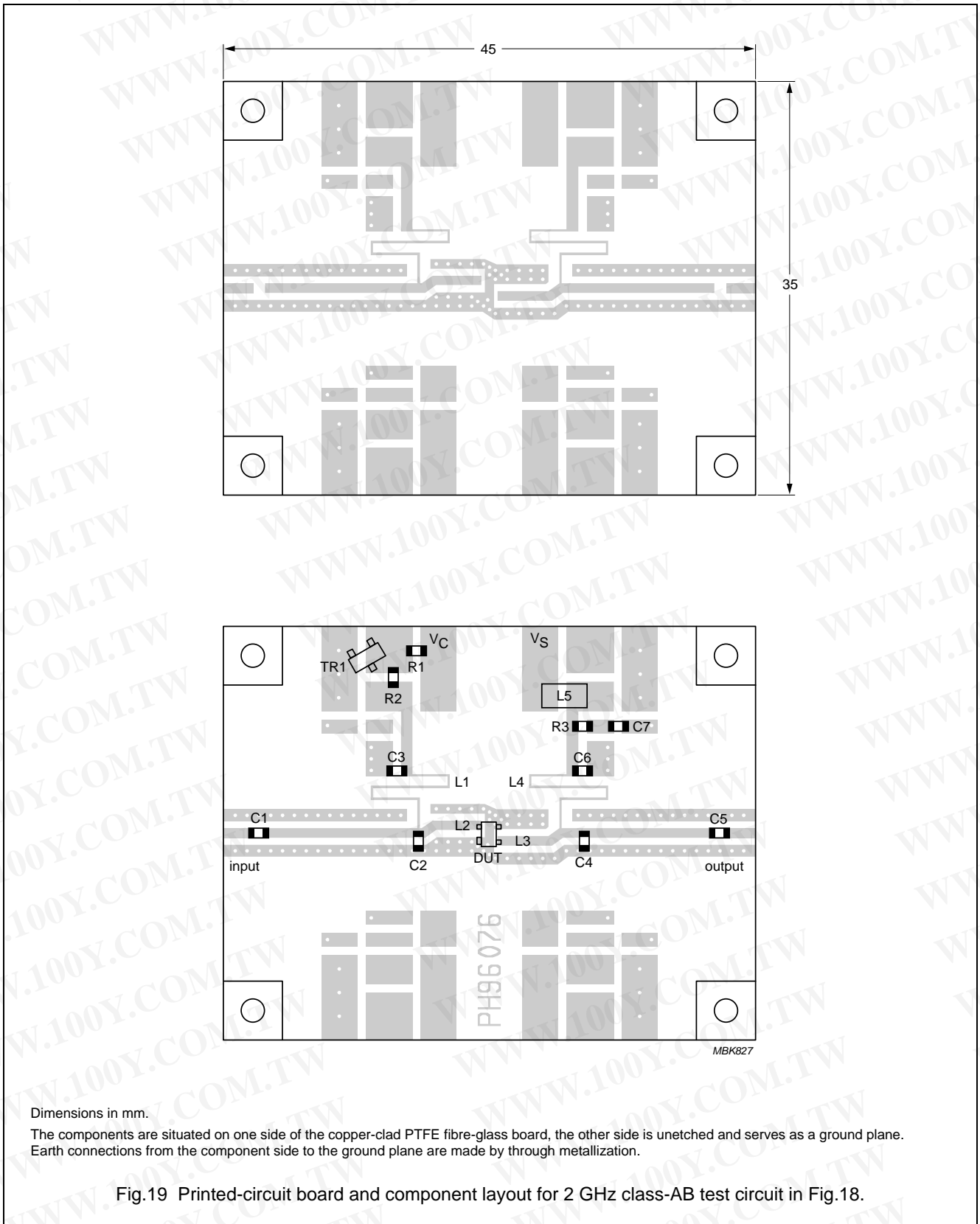
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C5	multilayer ceramic chip capacitor; note 1	24 pF		
C2, C4	multilayer ceramic chip capacitor; note 1	2 pF		
C3, C6	multilayer ceramic chip capacitor, note 1	15 pF		
C7	multilayer ceramic chip capacitor; note 1	1 nF		
L1, L4	stripline; note 2	100 Ω	18 x 0.2 mm	
L2	stripline; note 2	50 Ω	5 x 0.8 mm	
L3	stripline; note 2	50 Ω	6 x 0.8 mm	
L5	Grade 4S2 Ferroxcube chip bead			4330 030 36300
R1	metal film resistor	220 Ω; 0.4 W		
R2, R3	metal film resistor	10 Ω; 0.4 W		
TR1	NPN transistor	BC817		9335 895 20215

Notes

- American Technical Ceramics type 100A or capacitor of same quality.
- The striplines are on a double copper-clad printed-circuit board with PTFE fibre-glass dielectric ($\epsilon_r = 6.15$, $\tan \delta = 0.0019$); thickness 0.64 mm, copper cladding = 35 μm .

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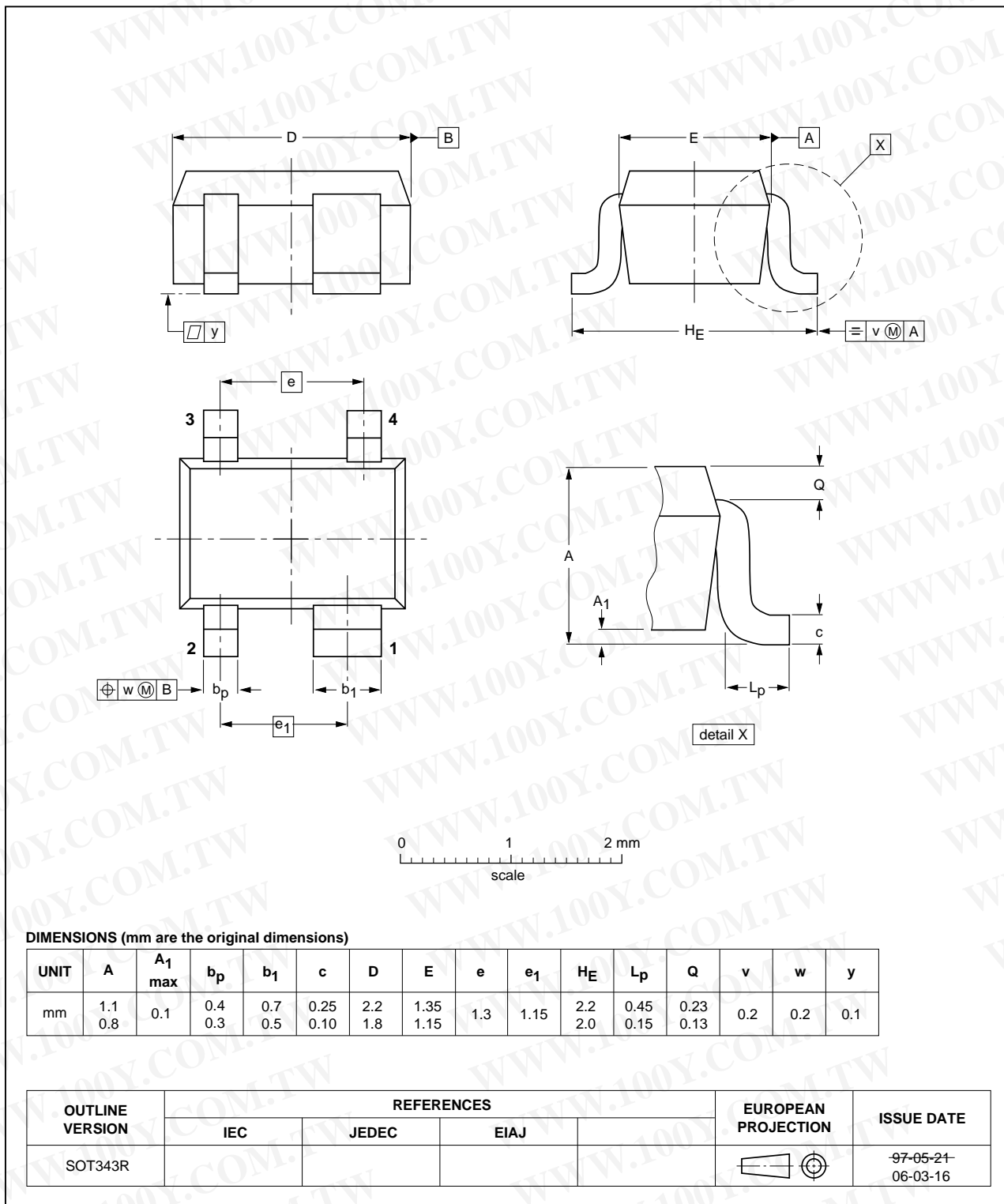
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PACKAGE OUTLINE

Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R



NPN wideband transistor

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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Customer notification

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Contact information

For additional information please visit: <http://www.nxp.com>

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