

# 74HCU04

Hex inverter

Rev. 3 — 16 September 2010

Product data sheet

## 1. General description

The 74HCU04 is high-speed Si-gate CMOS devices and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74HCU04 is a general purpose hex inverter. Each of the six inverters is a single stage.

## 2. Features and benefits

- Balanced propagation delays
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Ordering information

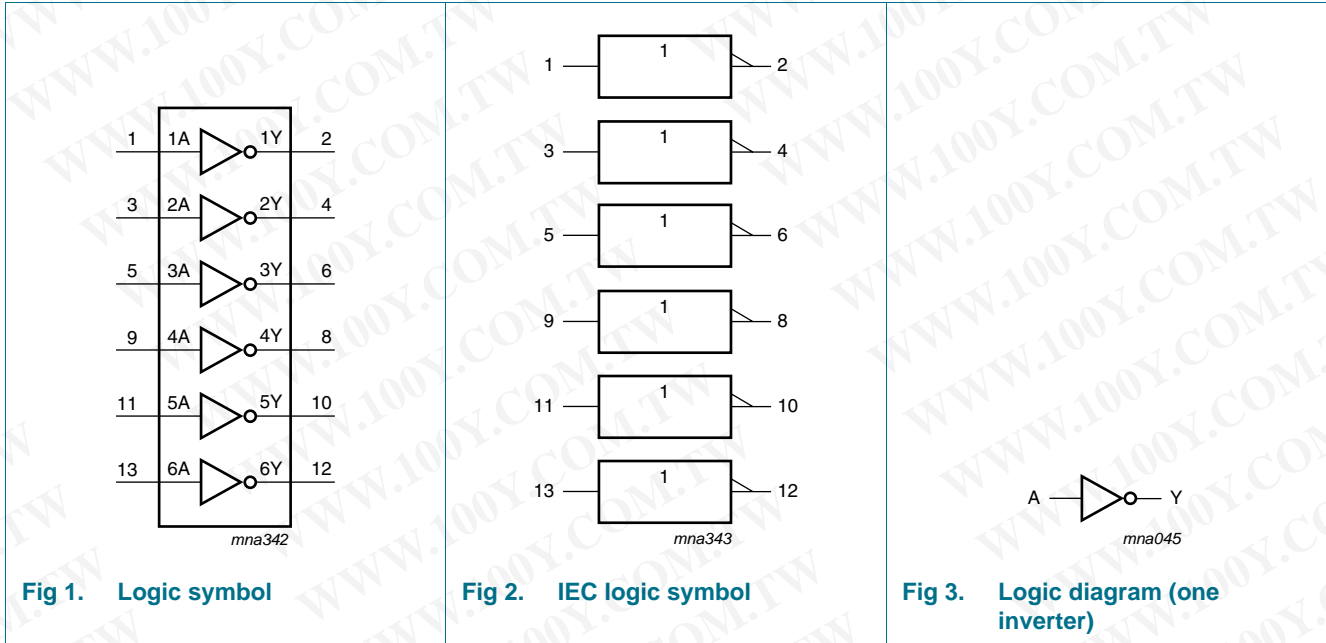
Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HCU04N	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCU04D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCU04DB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCU04PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCU04BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1

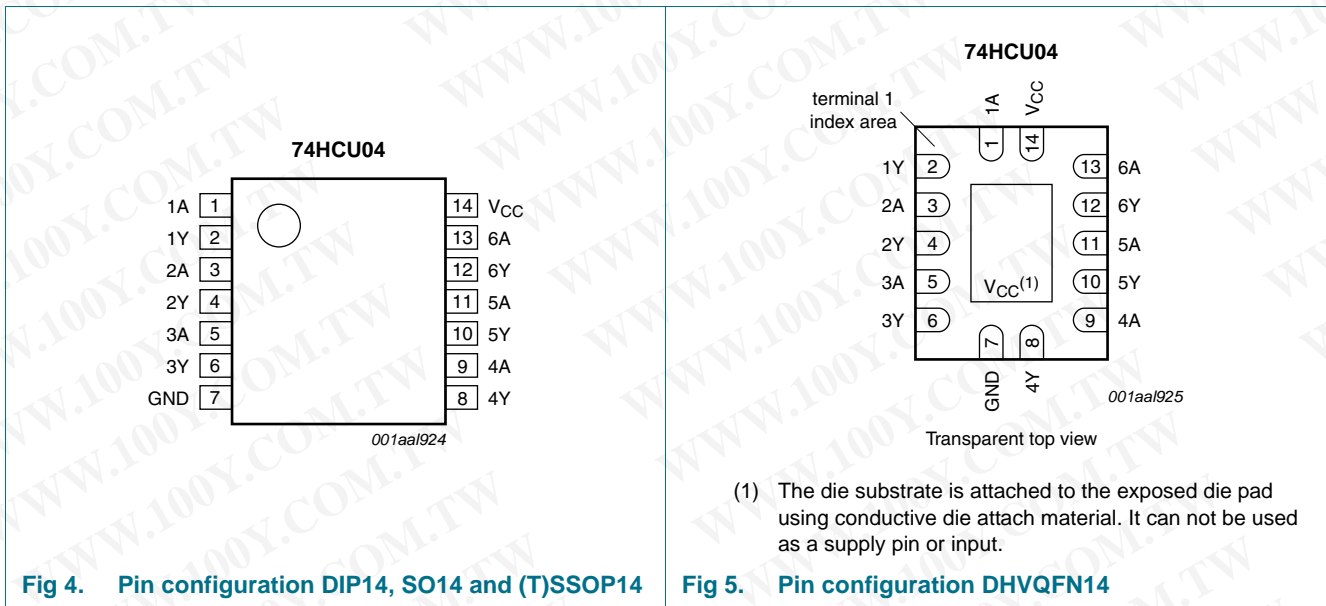
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4. Functional diagram



5. Pinning information



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## 5.1 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1Y	2	data output
2A	3	data input
2Y	4	data output
3A	5	data input
3Y	6	data output
GND	7	ground (0 V)
4Y	8	data output
4A	9	data input
5Y	10	data output
5A	11	data input
6Y	12	data output
6A	13	data input
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	nY
L	H
H	L

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	[1]	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1]	±50	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation		[2]		
	DIP14 package		-	750	mW
	SO14, (T)SSOP14 and DHVQFN14 packages		-	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] For DIP14 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.  
 For SO14 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
 For (T)SSOP14 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.  
 For DHVQFN14 packages:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C

## 9. Static characteristics

**Table 6. Static characteristics**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.7	1.4	-	1.7	-	1.7	-	V
		$V_{CC} = 3.0\text{ V}$	3.6	2.6	-	3.6	-	3.6	-	V
		$V_{CC} = 5.5\text{ V}$	4.8	3.4	-	4.8	-	4.8	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.6	0.3	-	0.3	-	0.3	V
		$V_{CC} = 3.0\text{ V}$	-	1.9	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5\text{ V}$	-	2.6	1.2	-	1.2	-	1.2	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -20\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.8	2.0	-	1.8	-	1.8	-	V
		$I_O = -20\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	4.0	4.5	-	4.0	-	4.0	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -20\ \mu\text{A}; V_{CC} = 6.0\text{ V}$	5.5	6.0	-	5.5	-	5.5	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 20\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.2	-	0.2	-	0.2	V
		$I_O = 20\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.5	-	0.5	-	0.5	V
		$I_O = 4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 20\ \mu\text{A}; V_{CC} = 6.0\text{ V}$	-	0	0.5	-	0.5	-	0.5	V
		$I_O = 5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V

**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu$ A
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	2	-	20	-	20	$\mu$ A
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 Voltages are referenced to GND (ground = 0 V); For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
$t_{pd}$	propagation delay	nA to nY; see <a href="#">Figure 6</a> <a href="#">[1]</a>					
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	19	70	90	105	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	7	14	18	21	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	5	-	-	-	ns
$t_t$	transition time	see <a href="#">Figure 6</a> <a href="#">[2]</a>					
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	19	75	95	110	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	7	15	19	22	ns
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	6	13	16	19	ns
$C_{PD}$	power dissipation capacitance	per inverter; $V_I = \text{GND to } V_{CC}$ <a href="#">[3]</a>	10	-			pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$ ,  $t_{PLH}$ .

[2]  $t_t$  is the same as  $t_{THL}$ ,  $t_{TLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

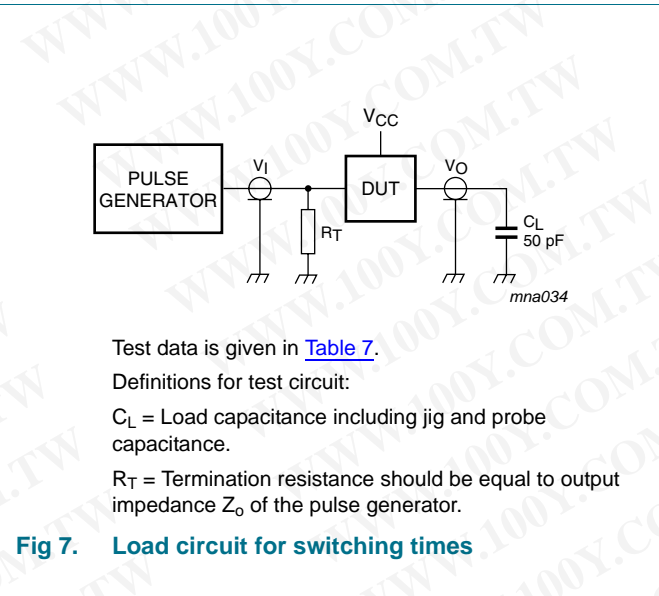
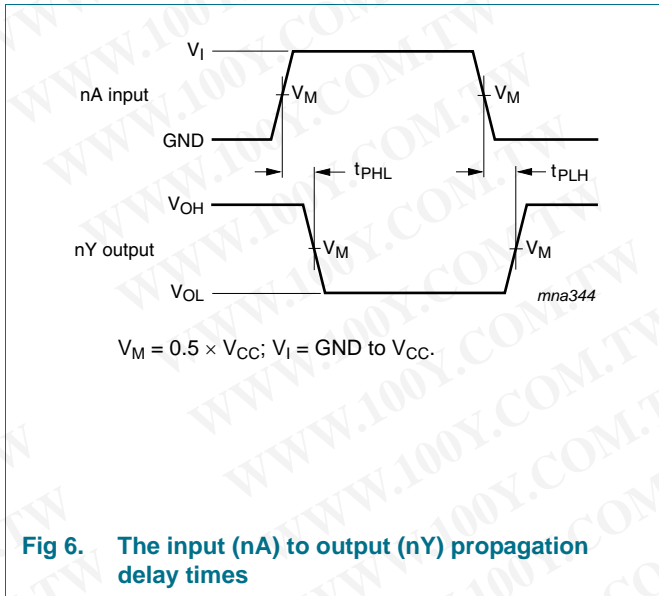
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

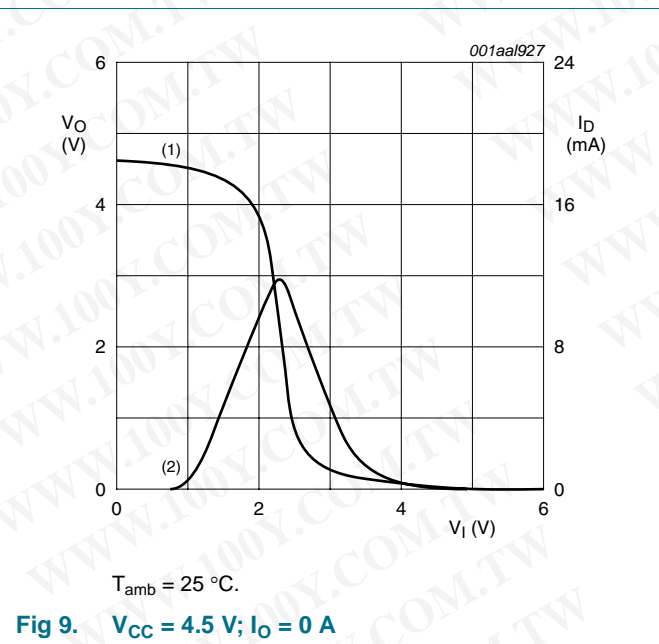
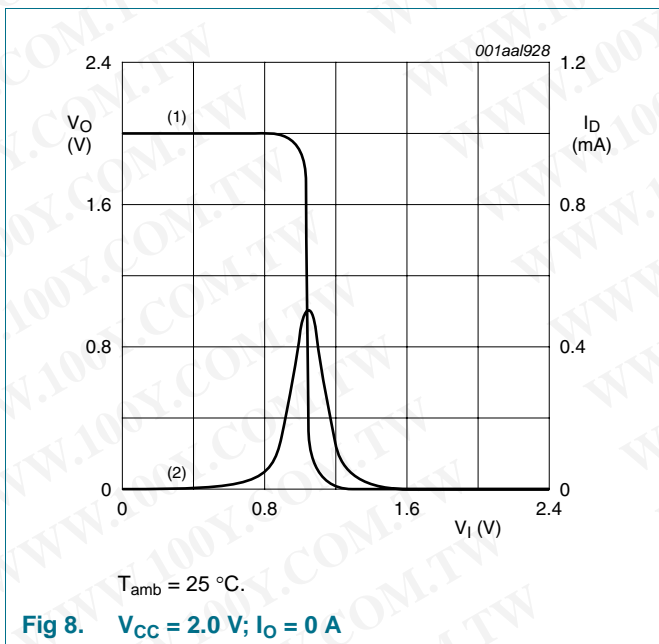
$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

11. Waveforms



12. Typical transfer characteristics



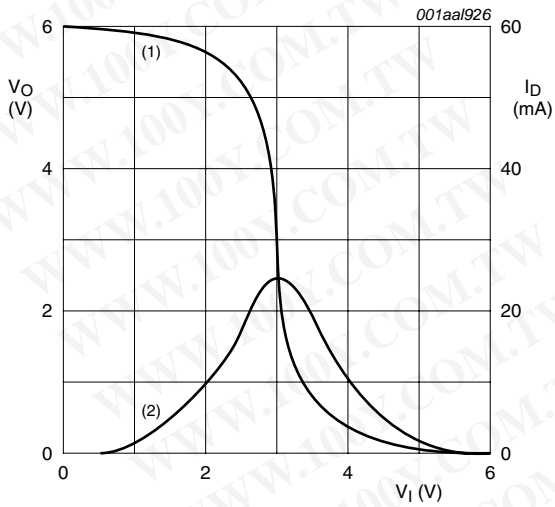
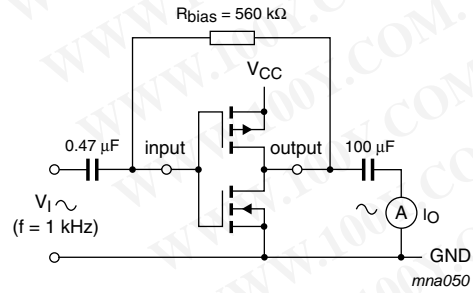


Fig 10.  $V_{CC} = 6.0\text{ V}$ ;  $I_O = 0\text{ A}$



$$g_{fs} = \frac{\Delta I_O}{\Delta V_i}$$

$f_i = 1\text{ kHz}$  at  $V_O$  is constant

Fig 11. Test set-up for measuring forward transconductance

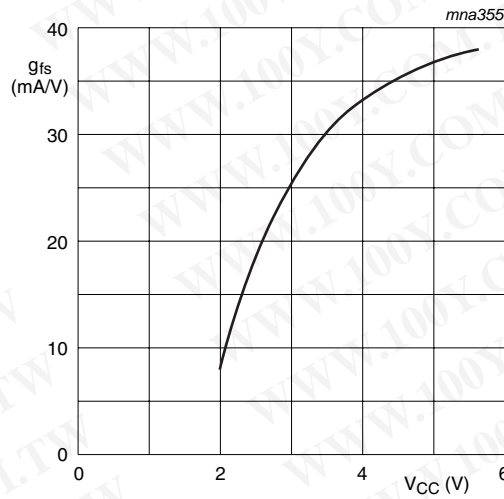


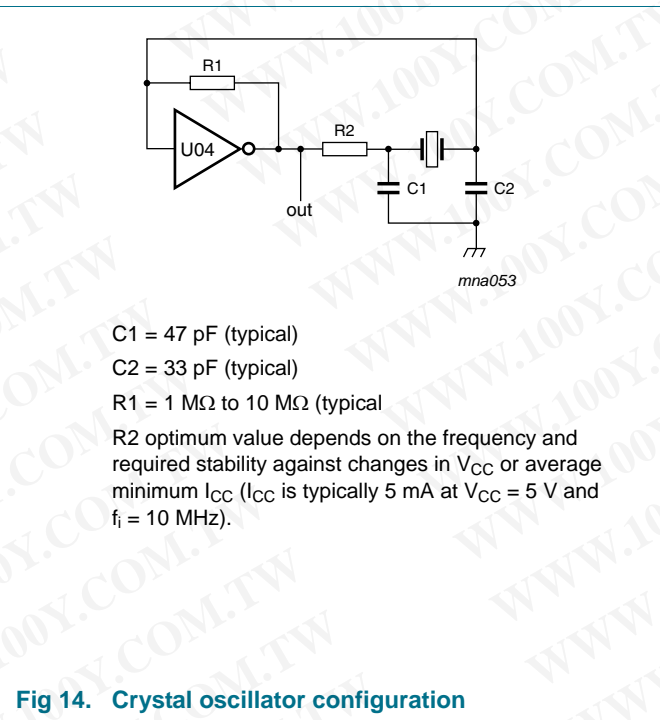
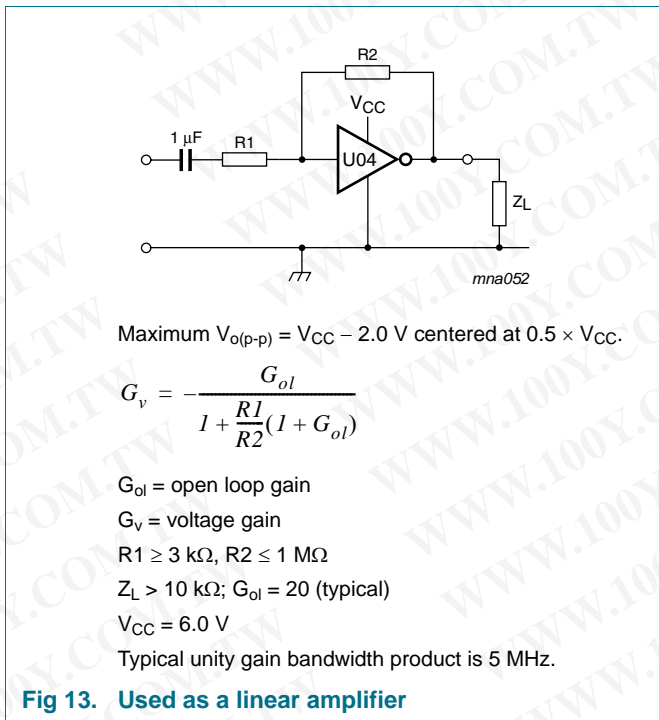
Fig 12. Typical forward transconductance as a function of the supply voltage

### 13. Application information

Some applications are:

- Linear amplifier (see [Figure 13](#))
- In crystal oscillator design (see [Figure 14](#))
- Astable multivibrator (see [Figure 15](#))

**Remark:** All values given are typical unless otherwise specified.



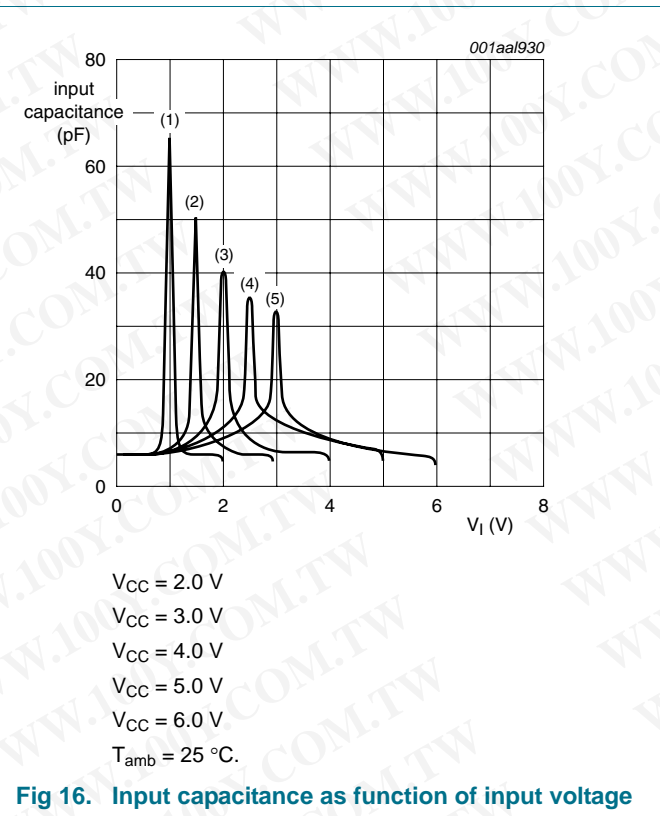
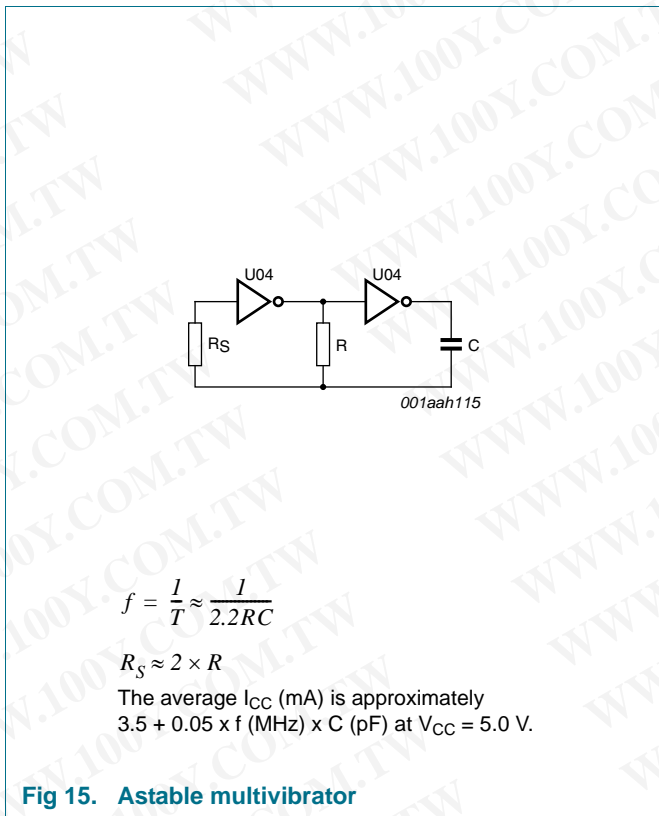
**Table 8. External components for resonator ( $f < 1 \text{ MHz}$ )**

All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 M $\Omega$	220 k $\Omega$	56 pF	20 pF
16 kHz to 24.9 kHz	22 M $\Omega$	220 k $\Omega$	56 pF	10 pF
25 kHz to 54.9 kHz	22 M $\Omega$	100 k $\Omega$	56 pF	10 pF
55 kHz to 129.9 kHz	22 M $\Omega$	100 k $\Omega$	47 pF	5 pF
130 kHz to 199.9 kHz	22 M $\Omega$	47 k $\Omega$	47 pF	5 pF
200 kHz to 349.9 kHz	10 M $\Omega$	47 k $\Omega$	47 pF	5 pF
350 kHz to 600 kHz	10 M $\Omega$	47 k $\Omega$	47 pF	5 pF

Table 9. Optimum value for R2

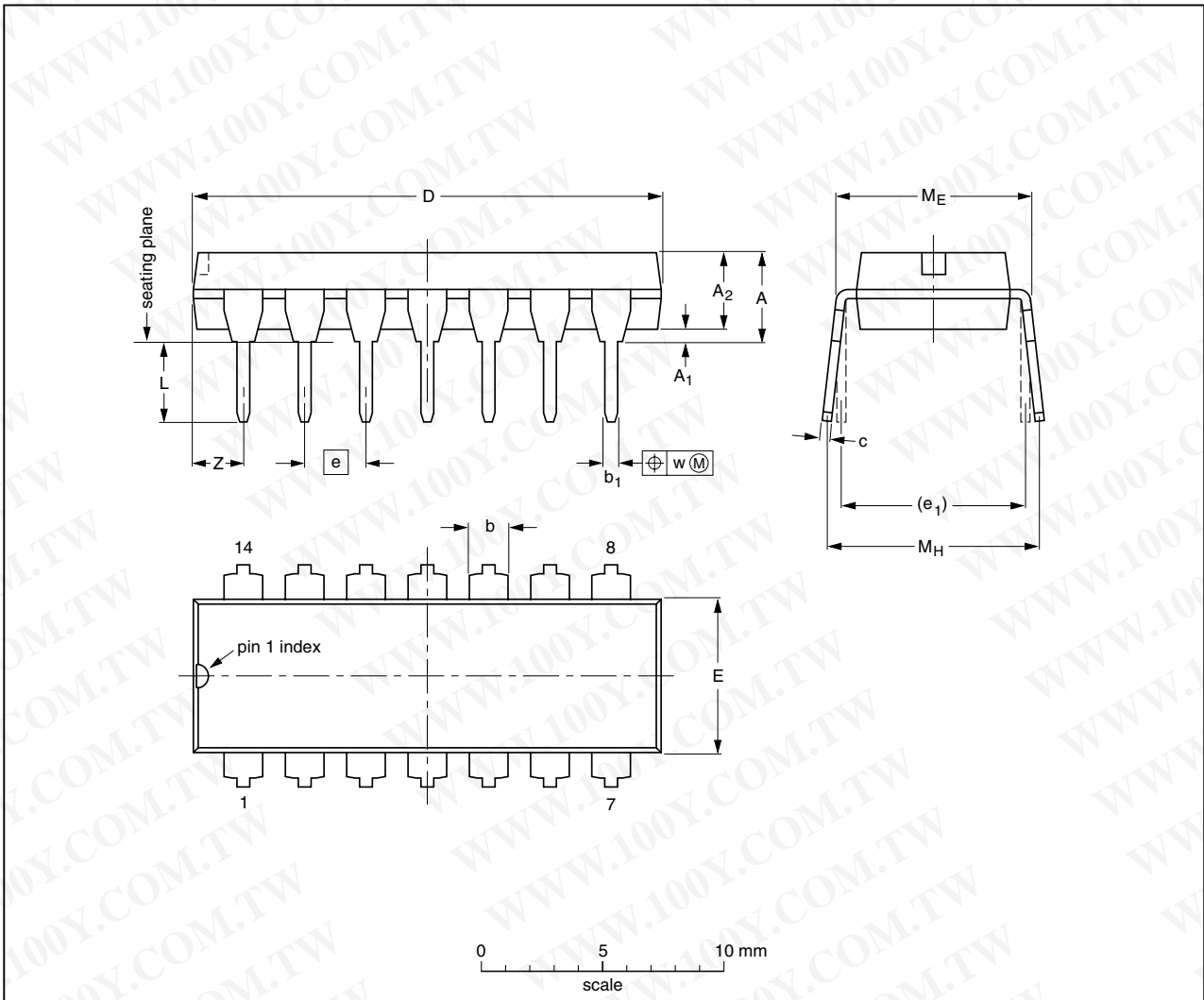
Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required I <sub>CC</sub>
	8.0 kΩ	minimum influence due to change in V <sub>CC</sub>
6 kHz	1.0 kΩ	minimum required I <sub>CC</sub>
	4.7 kΩ	minimum influence by V <sub>CC</sub>
10 kHz	0.5 kΩ	minimum required I <sub>CC</sub>
	2.0 kΩ	minimum influence by V <sub>CC</sub>
14 kHz	0.5 kΩ	minimum required I <sub>CC</sub>
	1.0 kΩ	minimum influence by V <sub>CC</sub>
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF



14. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT27-1	050G04	MO-001	SC-501-14		99-12-27 03-02-13

Fig 17. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

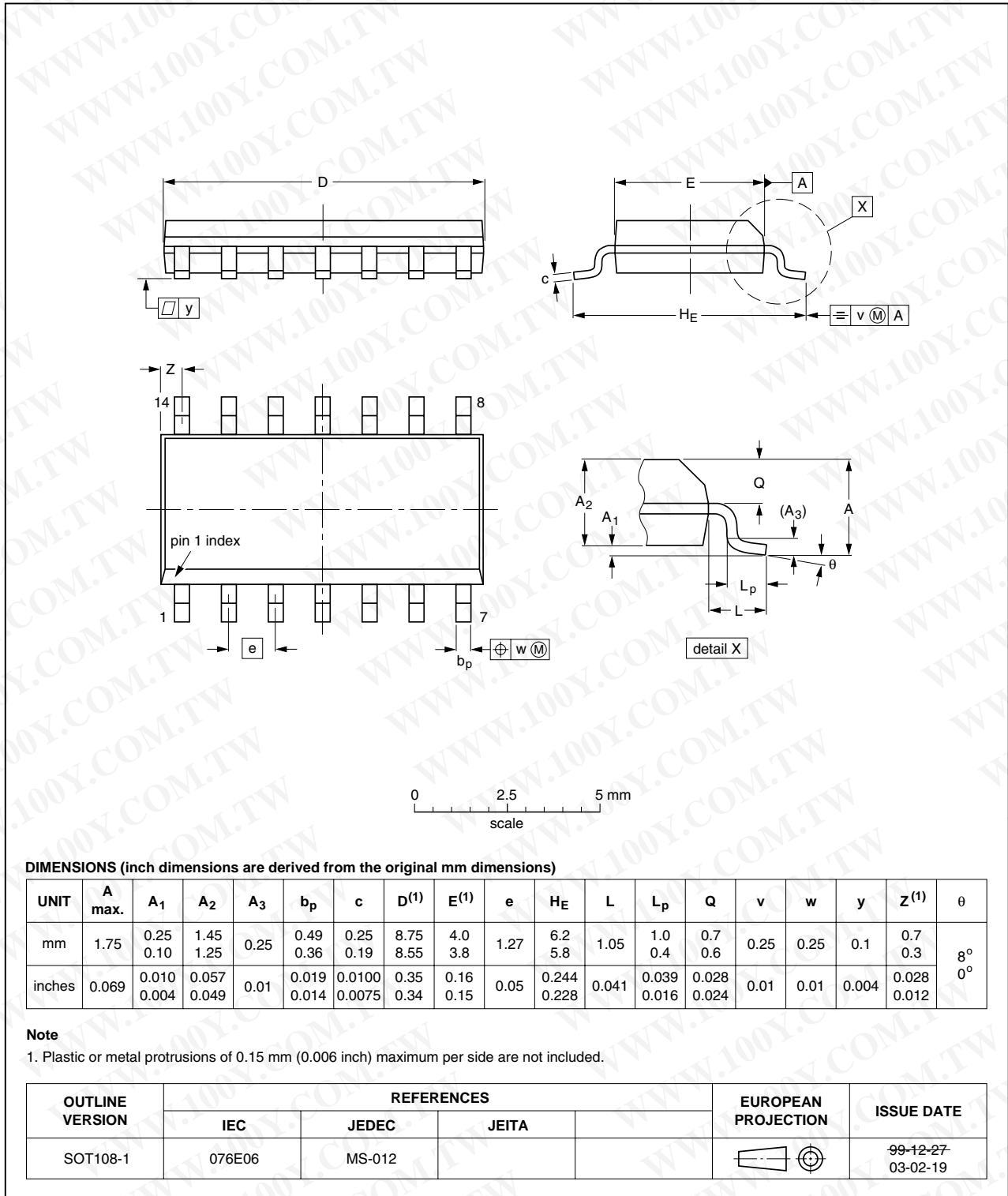


Fig 18. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

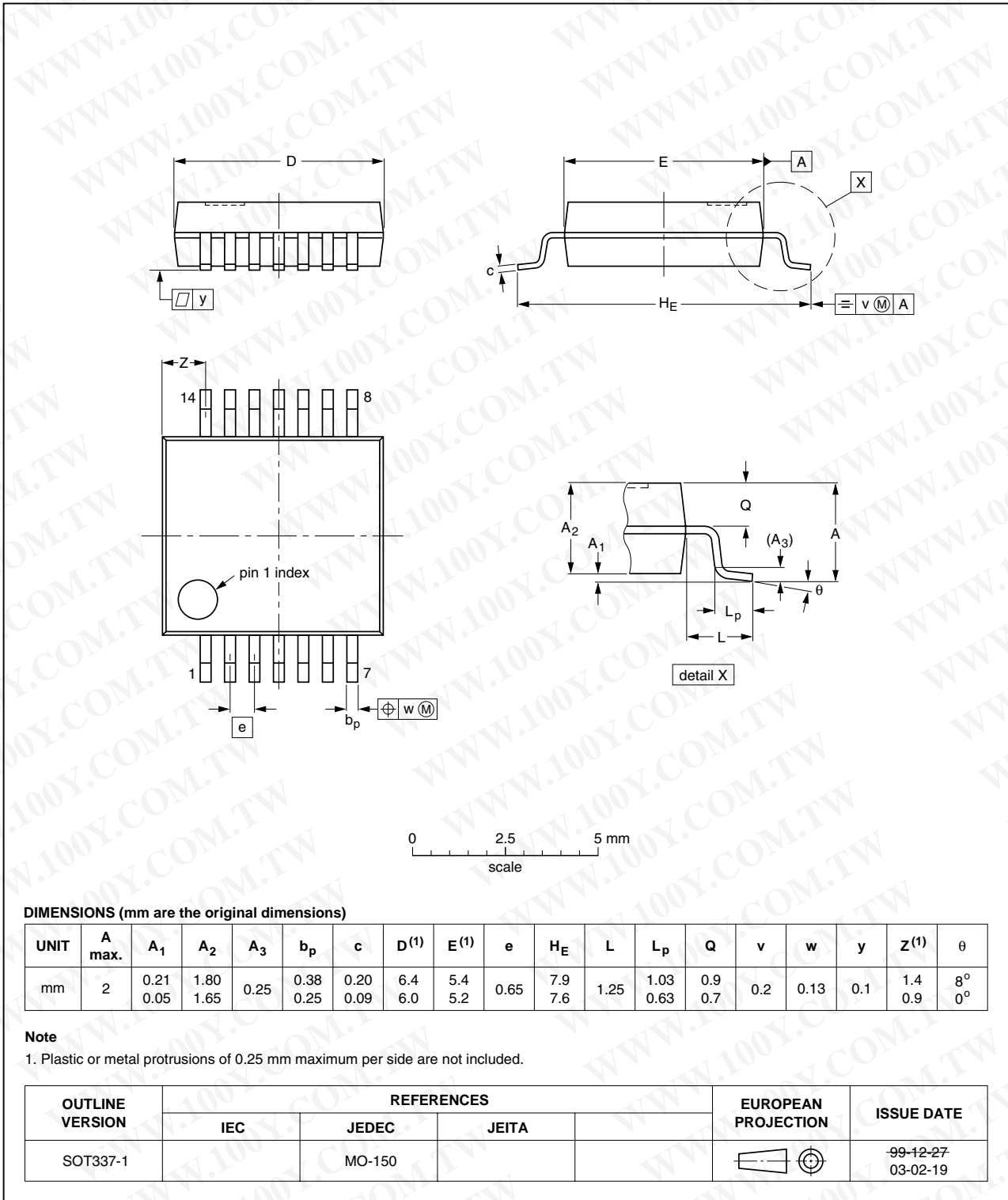


Fig 19. Package outline SOT337-1 (SSOP14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

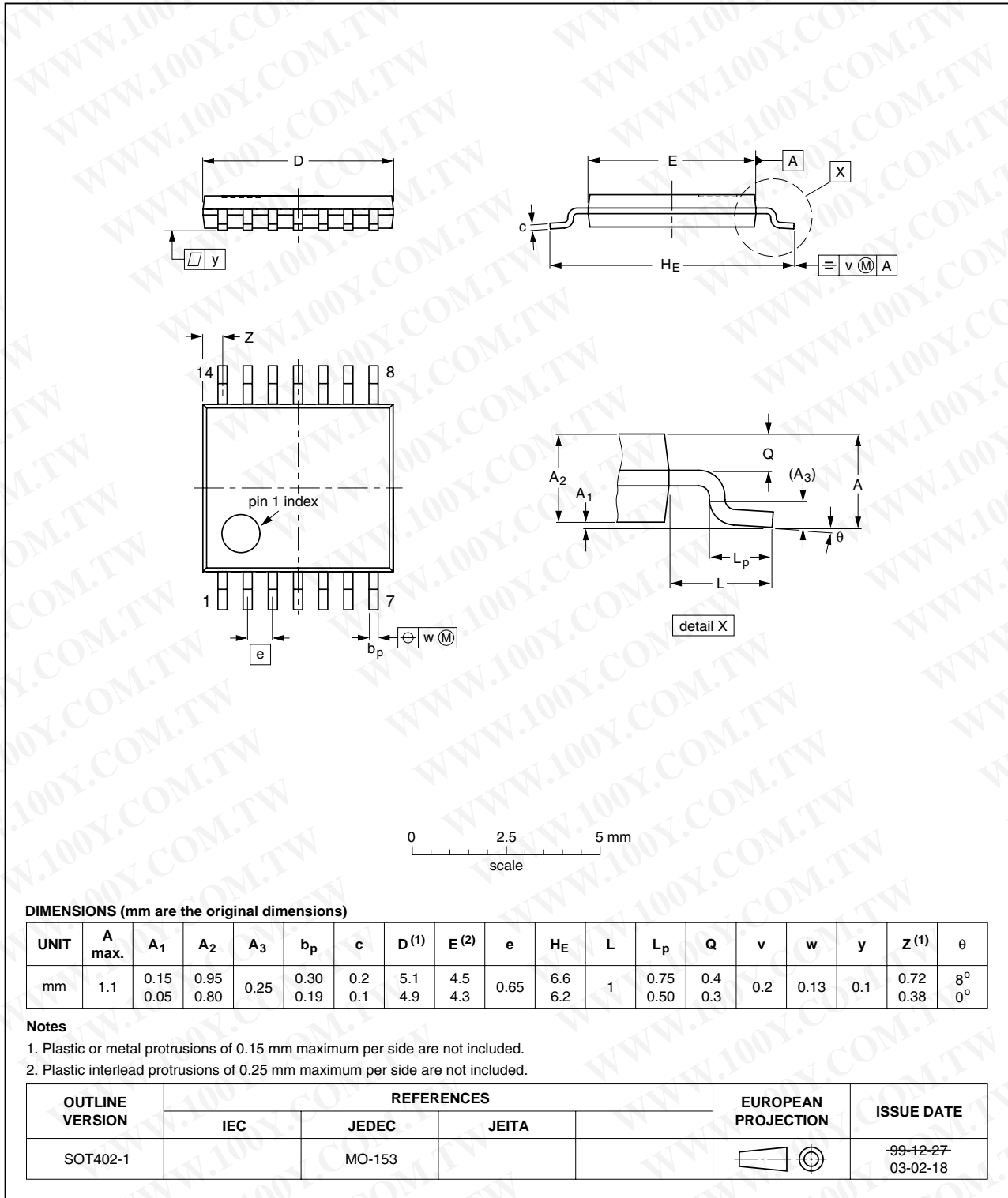


Fig 20. Package outline SOT402-1 (TSSOP14)



## 15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge Device Model
TTL	Transistor-Transistor Logic

## 16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCU04 v.3	20100916	Product data sheet	-	74HCU04_CNV v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 3</a>: DHVQFN14 package added.</li> <li><a href="#">Section 7</a>: derating values added for DHVQFN14 package.</li> <li><a href="#">Section 14</a>: outline drawing added for DHVQFN14 package.</li> </ul>			
74HCU04_CNV v.2	19970826	Product specification	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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