

MOS FIELD EFFECT POWER TRANSISTOR 2SJ302, 302-Z

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SJ302 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 0.1 \Omega$ ($V_{GS} = -10 \text{ V}$, $I_D = -8 \text{ A}$)
 $R_{DS(on)} \leq 0.24 \Omega$ ($V_{GS} = -4 \text{ V}$, $I_D = -6 \text{ A}$)
- Low C_{iss} $C_{iss} = 1200 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode

QUALITY GRADE

Standard

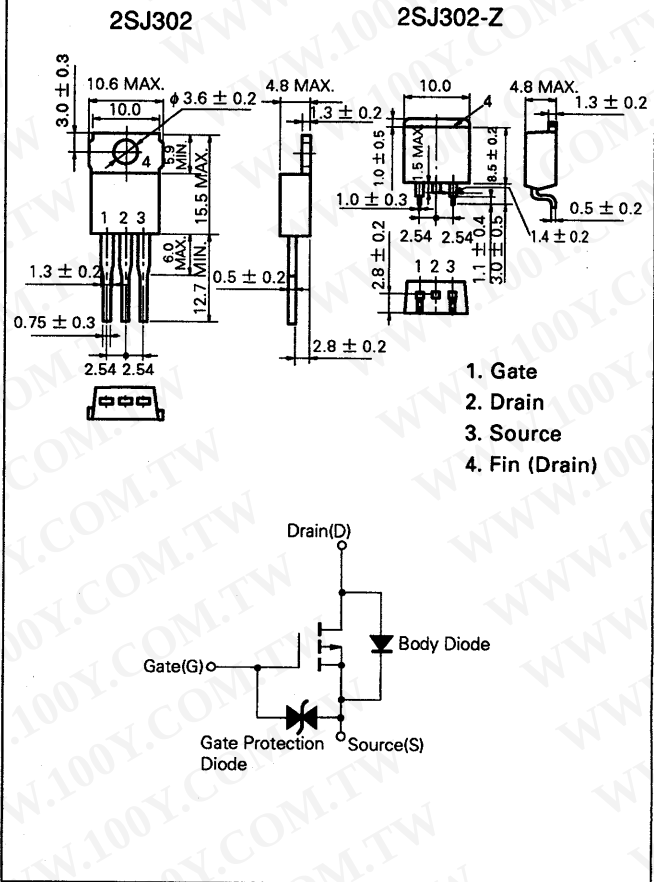
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DS}	-60	V
Gate to Source Voltage	V_{GS}	-20, +10	V
Drain Current (DC)	$I_{D(DC)}$	± 16	A
Drain Current (pulse)	$I_{D(pulse)*}$	± 64	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_T	75	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

PACKAGE DIMENSIONS in millimeters

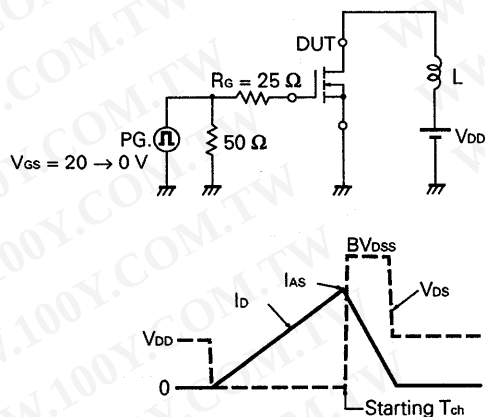


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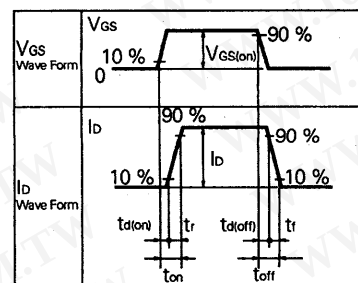
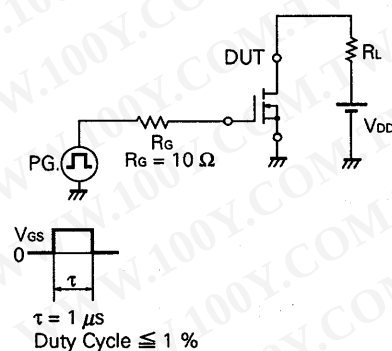
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		75	100	$\text{m}\Omega$	$V_{GS} = -10\text{ V}$, $I_D = -8\text{ A}$
Drain to Source On-state Resistance	$R_{DS(on)}$		130	240	$\text{m}\Omega$	$V_{GS} = -4.0\text{ V}$, $I_D = -6\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	-1.0		-2.0	V	$V_{DS} = -10\text{ V}$, $I_D = -1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	5.0			S	$V_{DS} = -10\text{ V}$, $I_D = -8\text{ A}$
Drain Leakage Current	I_{DSS}			-10	μA	$V_{DS} = -60\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 16\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		1200		pF	$V_{DS} = -10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		670		pF	
Reverse Transfer Capacitance	C_{rss}		290		pF	
Turn-On Delay Time	$t_{d(on)}$		30		ns	$V_{GS(on)} = -10\text{ V}$ $V_{DD} = -30\text{ V}$ $I_D = -8\text{ A}$, $R_G = 10\ \Omega$ $R_L = 3.75\ \Omega$
Rise Time	t_r		170		ns	
Turn-Off Delay Time	$t_{d(off)}$		150		ns	
Fall Time	t_f		130		ns	
Total Gate Charge	Q_G		42		nC	$V_{GS} = -10\text{ V}$ $I_D = -16\text{ A}$ $V_{DD} = -48\text{ V}$
Gate to Source Charge	Q_{GS}		3		nC	
Gate to Drain Charge	Q_{GD}		17		nC	
Diode Forward Voltage	V_{SD}		1.0		V	$I_F = -16\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		110		ns	$I_F = -16\text{ A}$, $V_{GS} = 0$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		220		nC	

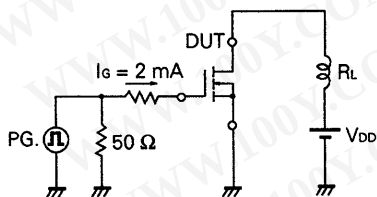
Test Circuit 1 : Avalanche Capability



Test Circuit 2 : Switching Time



Test Circuit 3 : Gate Charge

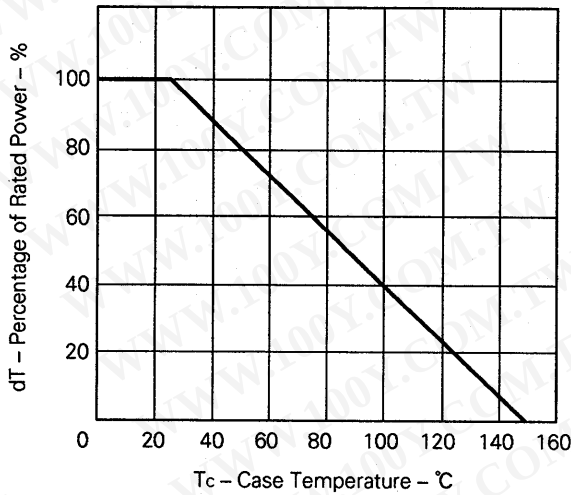


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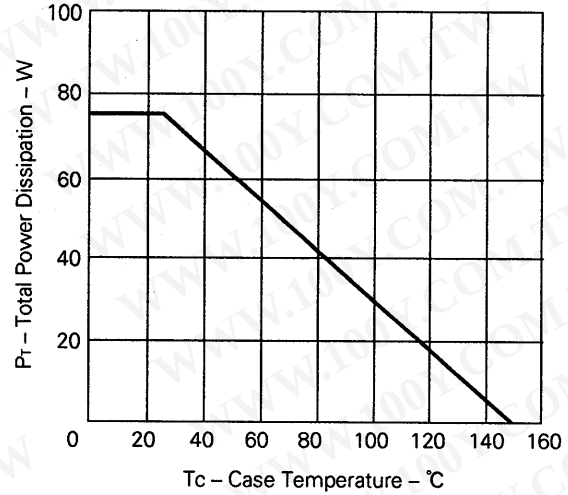
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TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

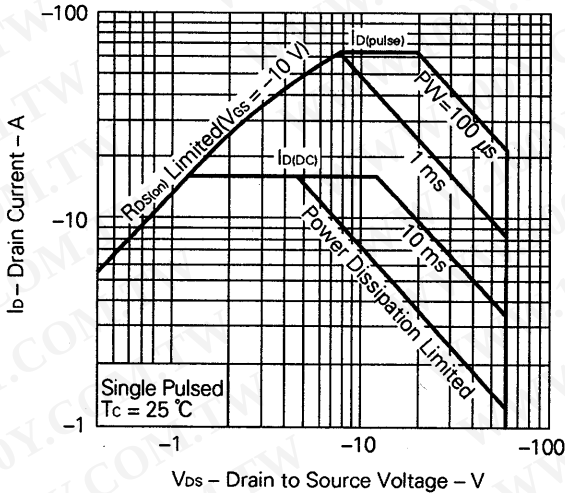
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



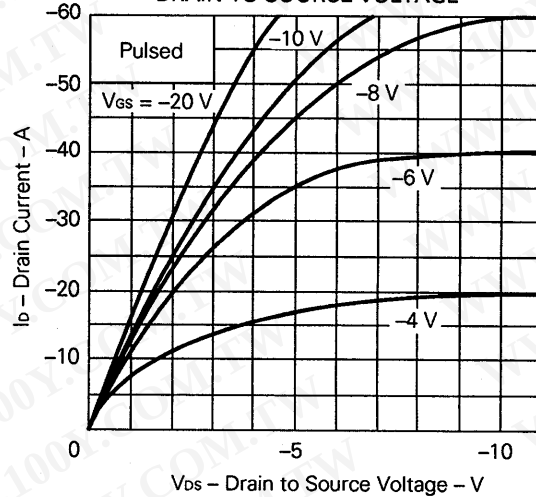
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE



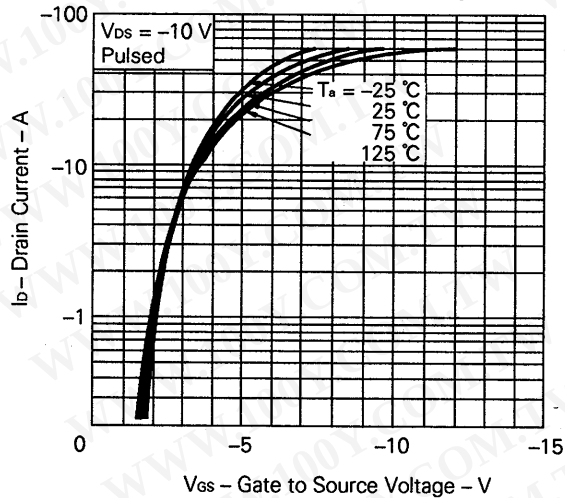
FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

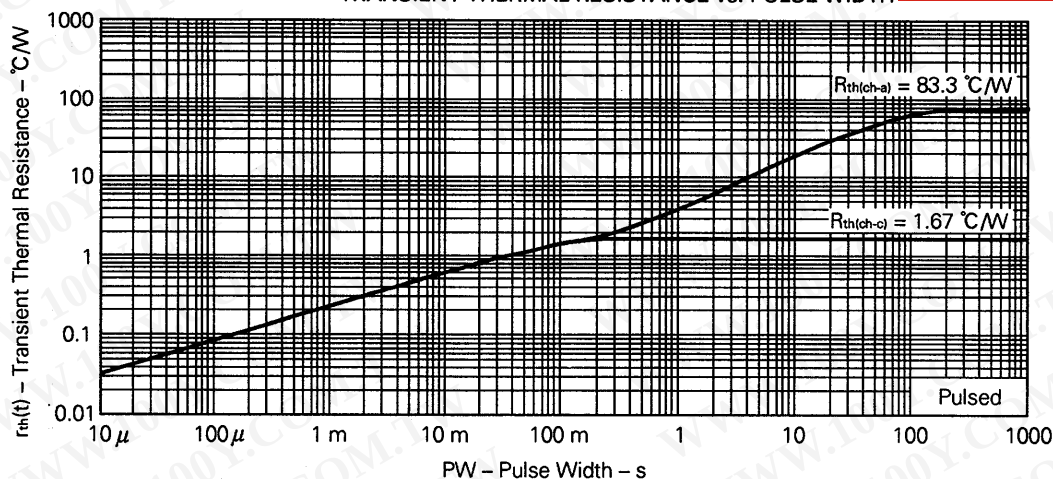


TRANSFER CHARACTERISTICS

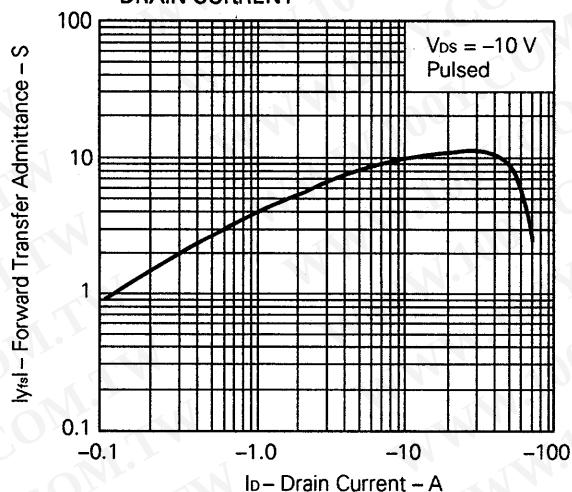


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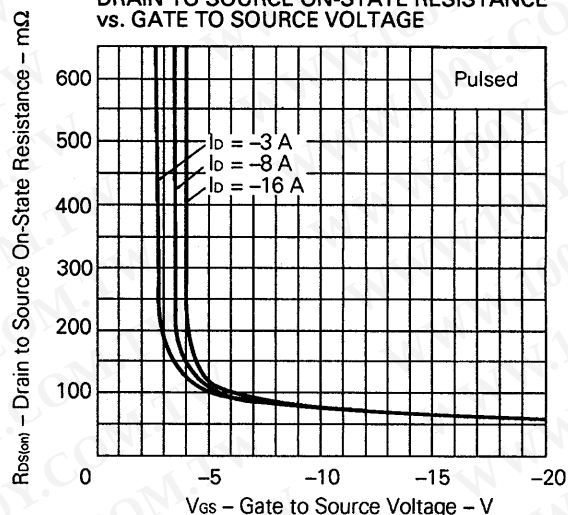
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



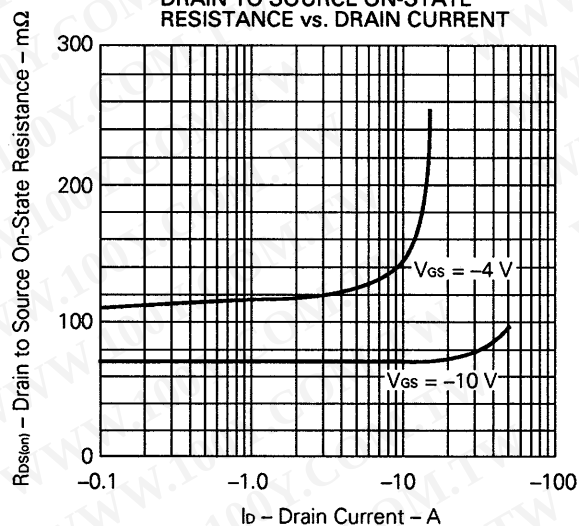
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



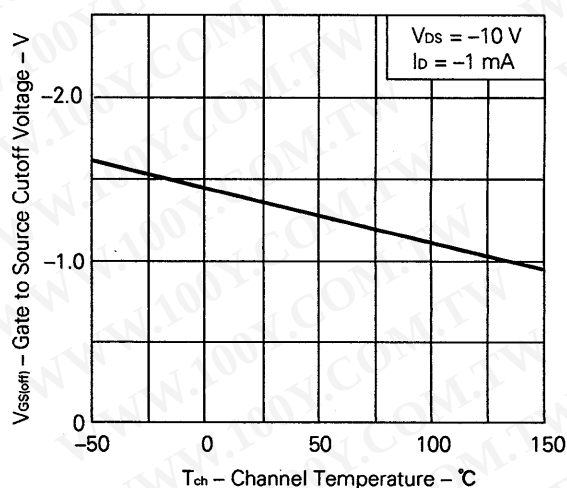
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

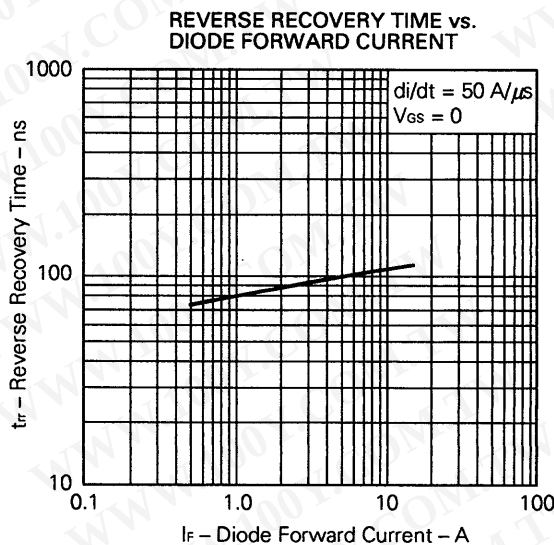
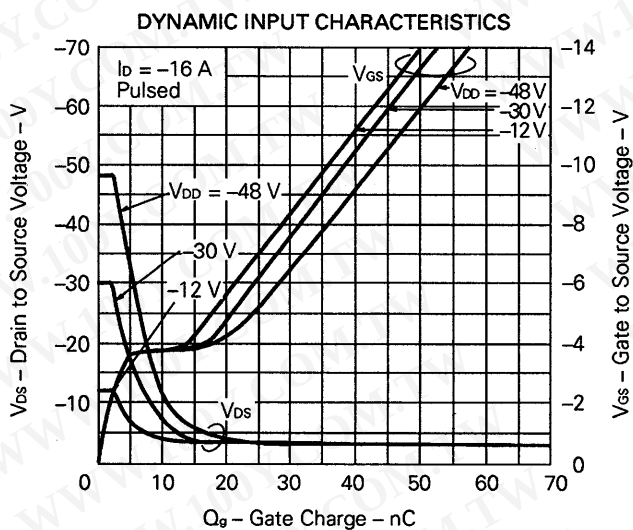
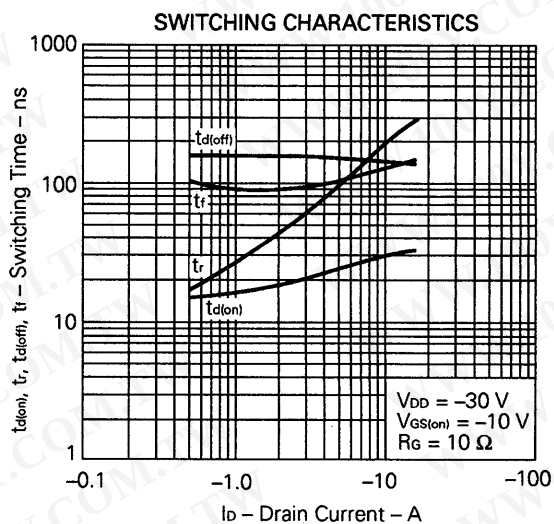
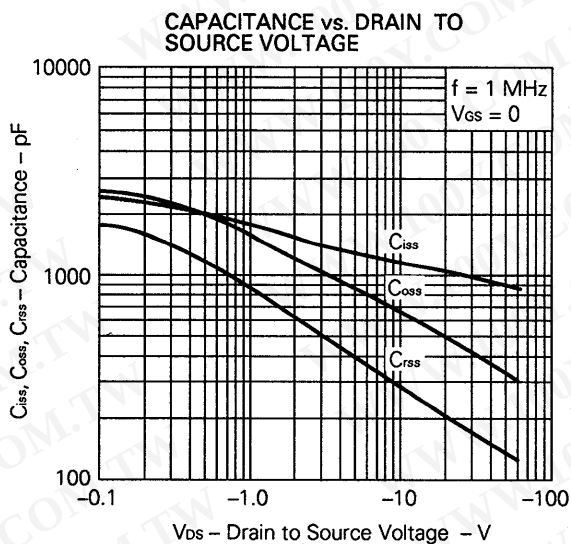
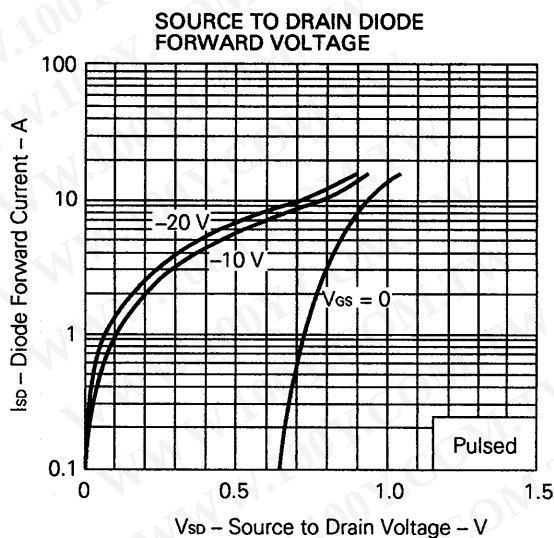
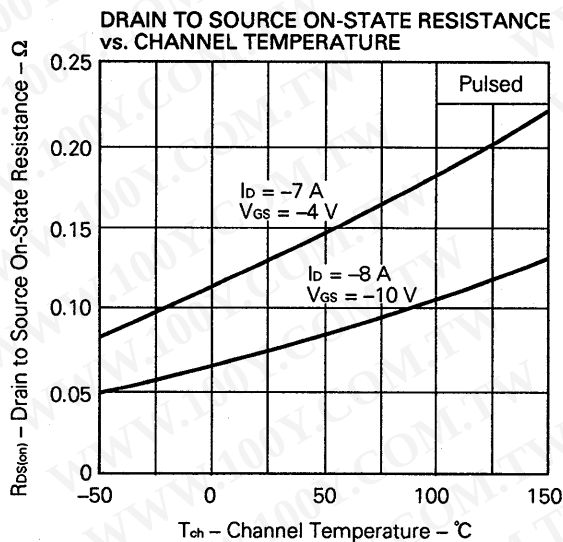


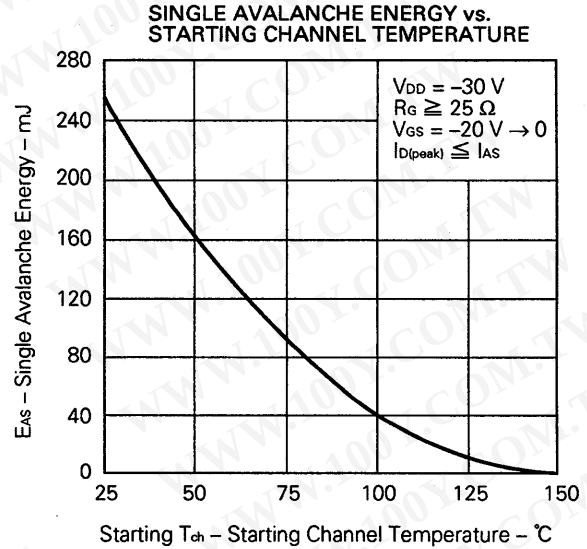
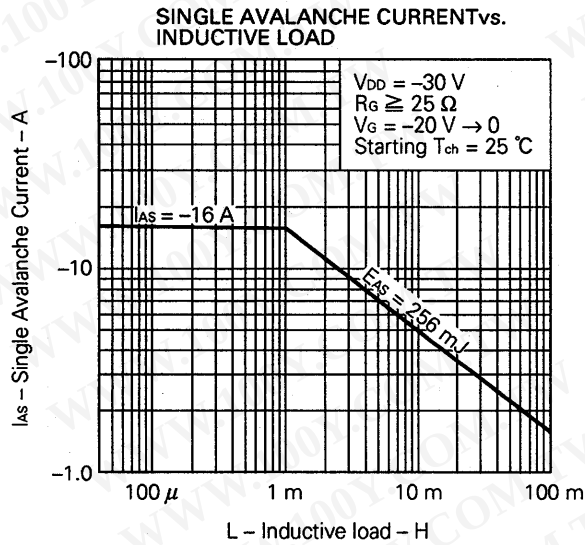
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







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Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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