File Number **2280**

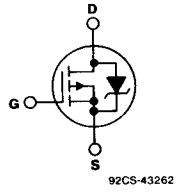
IRF9150, IRF9151

Power MOS Field-Effect Transistors P-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, 60 V and 100 V
$r_{DS(on)}$ = 0.150 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *Extreme device ruggedness*
- *Low on resistance*
- *High transconductance*
- *High input impedance*

P-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

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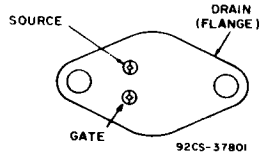
The IRF9150 and IRF9151 are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The P-channel IRF9150 is an approximate electrical complement to the N-channel IRF150.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

TERMINAL DESIGNATION



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

		IRF9150		IRF9151	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-100		-60	V
CONTINUOUS DRAIN CURRENT @ T_C = 25°C	I_D		-25		A
CONTINUOUS DRAIN CURRENT @ T_C = 100°C	I_D		-18		A
PULSE DRAIN CURRENT	I_{DM}		-100		A
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
MAX. POWER DISSIPATION @ T_C = 25°C	P_D		150 (See Fig. 18)		W
LINEAR DERATING FACTOR			1.2		W/°C
SINGLE-PULSE AVALANCHE ENERGY ③	E_{as}		1300 (See Fig. 14)		mJ
AVALANCHE CURRENT (REPETITIVE OR NONREPETITIVE)	I_{AR}		-25		A
OPERATING JUNCTION AND	T_J				°C
STORAGE TEMPERATURE RANGE	T_{stg}		-55 to +150		°C
LEAD TEMPERATURE (0.063 in. [1.6mm] from case for 10 s)			300		°C

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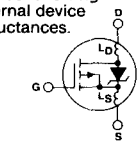
ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTICS		LIMITS TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRF9150	-100	—	—	V	V_{GS} = 0 V
		IRF9151	-60	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	All	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	All	—	—	-100	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	All	—	—	100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	All	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_J = 125°C
On-State Drain Current ①	$I_{D(on)}$	All	-25	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max}$, V_{GS} = 10 V
Static Drain-Source On-State Resistance ①	$r_{DS(on)}$	All	—	0.09	0.15	Ω	V_{GS} = -10 V, I_D = -10 A
Forward Transconductance ①	g_{fs}	All	4	10	—	S	V_{DS} = -10 V, I_D = -12.5 A
Input Capacitance	C_{iss}	All	—	2400	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	All	—	850	—	pF	
Reverse Transfer Capacitance	C_{rss}	All	—	400	—	pF	
Turn-On Delay Time	$t_{d(on)}$	All	—	16	24	ns	V_{DD} = -50 V, I_D = -25 A R_G = 6.8 Ω, R_D = 2 Ω See Figs. 16 and 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	All	—	110	160	ns	
Turn-Off Delay Time	$t_{d(off)}$	All	—	65	100	ns	
Fall Time	t_f	All	—	46	70	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	All	—	82	120	nC	V_{GS} = -10 V, I_D = -25 A, V_{DS} = 0.8 Max. Rating. See Figs. 11 and 19 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	All	—	14	21	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	All	—	42	65	nC	
Internal Drain Inductance	L_D	All	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
Internal Source Inductance	L_S	All	—	13	—	nH	Measured from the source pin, 6mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

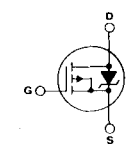


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	All	—	—	0.83	°C/W	
Case-to-Sink	$R_{\theta CS}$	All	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased
Junction-to-Ambient	$R_{\theta JA}$	All	—	—	30	°C/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode) ②	I_S	All	—	—	-25	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
Pulse Source Current (Body Diode) ③	I_{SM}	All	—	—	-100	A	
Diode Forward Voltage ②	V_{SD}	All	—	0.9	1.5	V	T_J = 25°C, I_S = 25 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	All	—	150	300	ns	T_J = 25°C, I_F = 25 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	All	0.30	0.70	1.5	μC	T_J = 25°C, I_F = 25 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	All	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
② Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
③ V_{DD} = 25 V, Starting T_J = 25°C, L = 3.2 mhy, I_{peak} = 25 A, R_{gs} = 25 Ω (See Figs. 14 & 15).

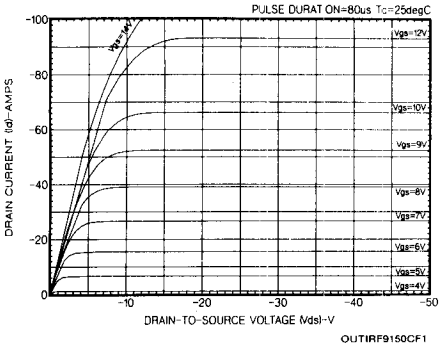


Fig. 1 - Typical output characteristics.

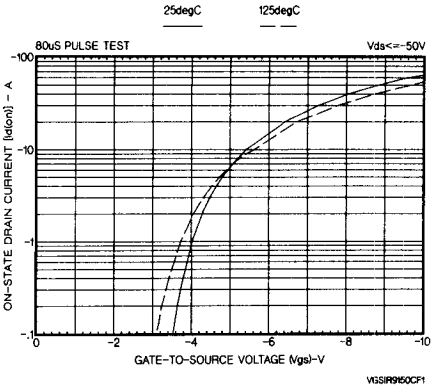


Fig. 2 - Typical transfer characteristics.

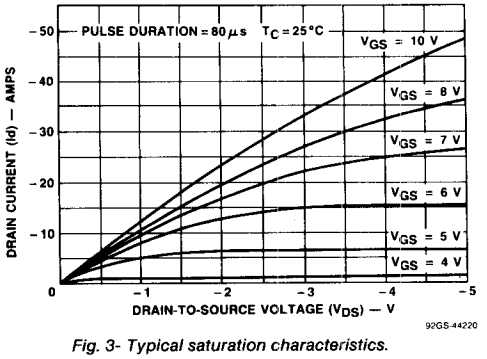


Fig. 3- Typical saturation characteristics.

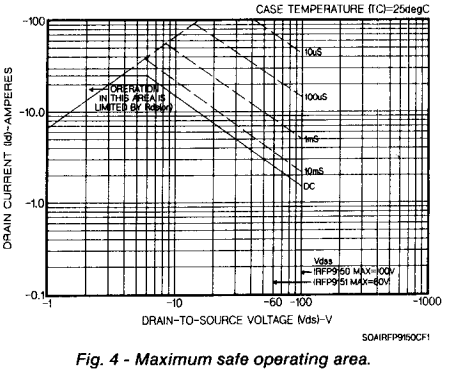


Fig. 4 - Maximum safe operating area.

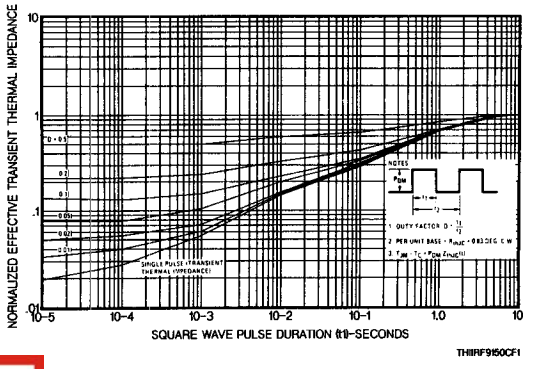


Fig. 5 - Maximum effective transient thermal impedance.

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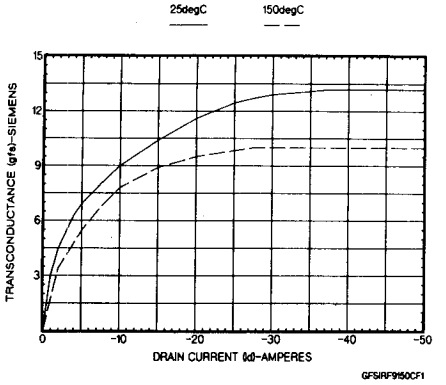

Fig. 6 - Typical transconductance vs. drain current.

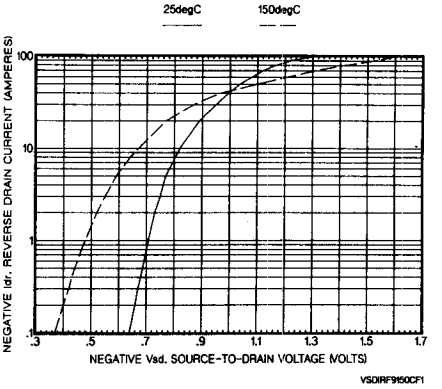

Fig. 7 - Typical source-drain diode forward voltage.

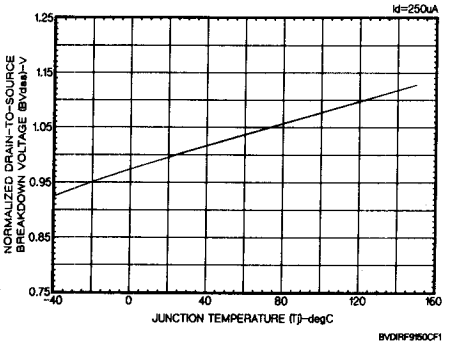

Fig. 8 - Normalized breakdown voltage vs. temperature.

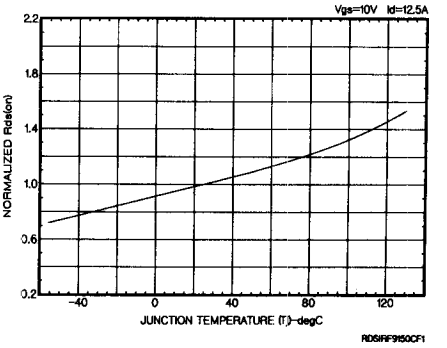

Fig. 9 - Normalized on-resistance vs. temperature.

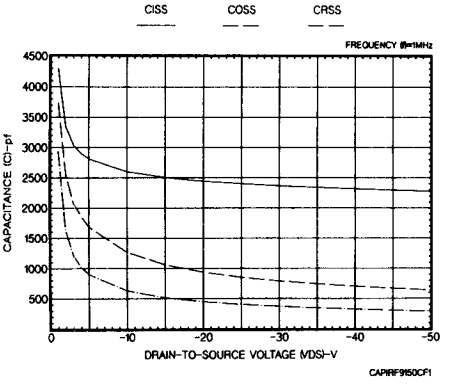

Fig. 10 - Typical capacitance vs. drain-to source voltage.

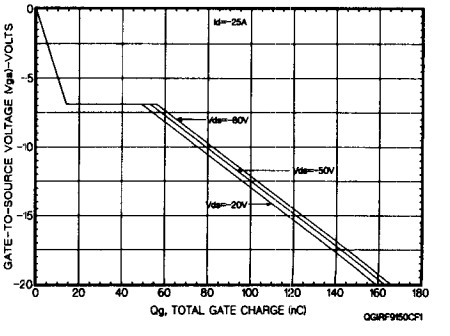

Fig. 11 - Typical gate charge vs. gate-to source voltage.

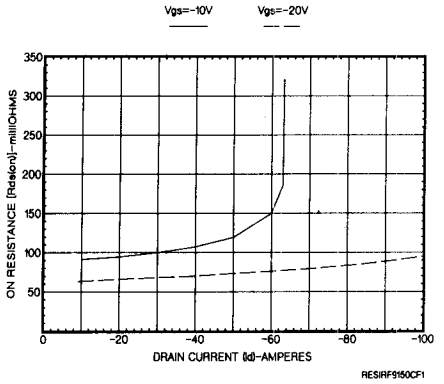

Fig. 12 - Typical on-resistance vs. drain current.

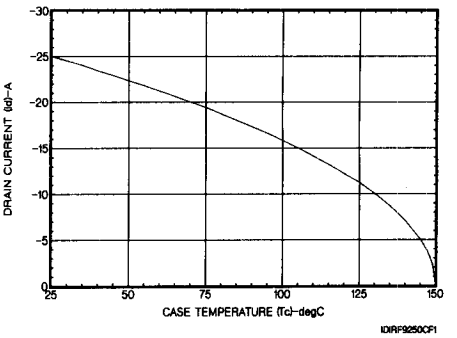

Fig. 13 - Maximum drain current vs. case temperature.

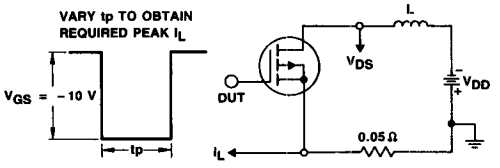

Fig. 14 - Unclamped inductive test circuit.

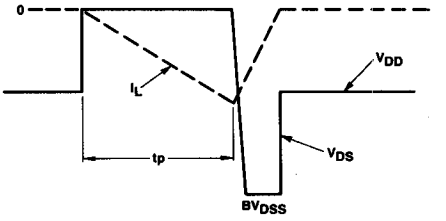

Fig. 15 - Unclamped inductive waveforms.

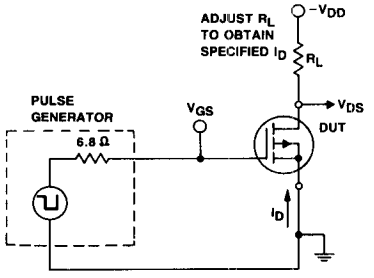

Fig. 16 - Switching time test circuit.

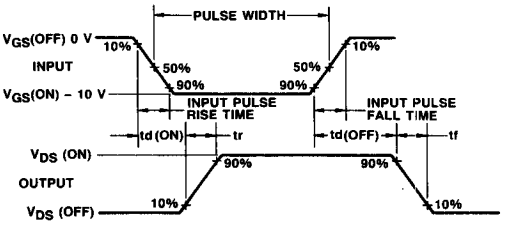

Fig. 17 - Switching time waveforms.

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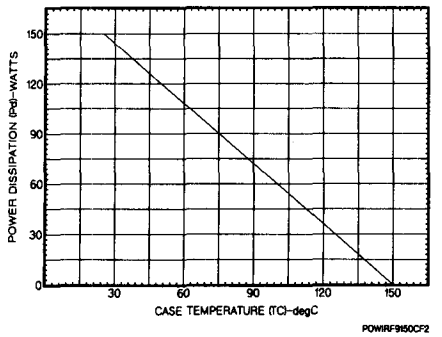

Fig. 18 - Power vs. temperature derating curve.

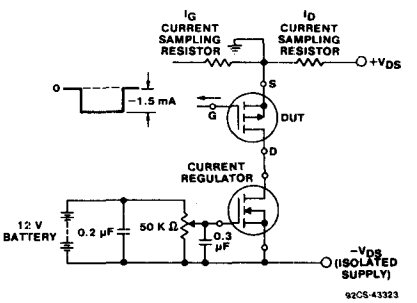

Fig. 19 - Gate charge test circuit.