International
IOR Rectifier

PD - 94266

# SMPS MOSFET

# IRLR3714
# IRLU3714

HEXFET® Power MOSFET

| $V_{DSS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|
| 20V | 20mΩ | 36A |

## Applications

- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Computer Processor Power

## Benefits

- Ultra-Low Gate Impedance
- Very Low $R_{DS(on)}$ at 4.5V $V_{GS}$
- Fully Characterized Avalanche Voltage and Current

D-Pak IRLR3714 | I-Pak IRLU3714

## Absolute Maximum Ratings

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 20 | V |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 36 ⑤ | A |
| $I_D$ @ $T_C$ = 70°C | Continuous Drain Current, $V_{GS}$ @ 10V | 31 | |
| $I_{DM}$ | Pulsed Drain Current① | 140 | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation③ | 47 | W |
| $P_D$ @$T_C$ = 70°C | Maximum Power Dissipation③ | 33 | W |
| | Linear Derating Factor | 0.31 | W/°C |
| $T_J$ , $T_{STG}$ | Junction and Storage Temperature Range | -55 to + 175 | °C |

## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | — | 3.2 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount)④ | — | 110 | |

Notes ① through ⑤ are on page 10

## Static @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 20 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.022 | — | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 15 | 20 | mΩ | $V_{GS}$ = 10V, $I_D$ = 18A ③ |
| | | — | 21 | 28 | | $V_{GS}$ = 4.5V, $I_D$ = 14A ③ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | — | 3.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 20 | µA | $V_{DS}$ = 16V, $V_{GS}$ = 0V |
| | | — | — | 100 | | $V_{DS}$ = 16V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 200 | nA | $V_{GS}$ = 16V |
| | Gate-to-Source Reverse Leakage | — | — | -200 | | $V_{GS}$ = -16V |

## Dynamic @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $g_{fs}$ | Forward Transconductance | 17 | — | — | S | $V_{DS}$ = 10V, $I_D$ = 14A |
| $Q_g$ | Total Gate Charge | — | 6.5 | 9.7 | nC | $I_D$ = 14A |
| $Q_{gs}$ | Gate-to-Source Charge | — | 1.8 | — | | $V_{DS}$ = 10V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | 2.9 | — | | $V_{GS}$ = 4.5V |
| $Q_{oss}$ | Output Gate Charge | — | 7.1 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 10V |
| $t_{d(on)}$ | Turn-On Delay Time | — | 8.7 | — | ns | $V_{DD}$ = 10V |
| $t_r$ | Rise Time | — | 78 | — | | $I_D$ = 14A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 10 | — | | $R_G$ = 1.8Ω |
| $t_f$ | Fall Time | — | 4.5 | — | | $V_{GS}$ = 4.5V ③ |
| $C_{iss}$ | Input Capacitance | — | 670 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 470 | — | | $V_{DS}$ = 10V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 68 | — | | $f$ = 1.0MHz |

## Avalanche Characteristics

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $E_{AS}$ | Single Pulse Avalanche Energy② | — | 72 | mJ |
| $I_{AR}$ | Avalanche Current① | — | 14 | A |

## Diode Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | 36⑤ | — | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | 140 | — | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.3 | V | $T_J$ = 25°C, $I_S$ = 18A, $V_{GS}$ = 0V ③ |
| | | — | 0.88 | — | | $T_J$ = 125°C, $I_S$ = 18A, $V_{GS}$ = 0V ③ |
| $t_{rr}$ | Reverse Recovery Time | — | 35 | 53 | ns | $T_J$ = 25°C, $I_F$ = 18A, $V_R$=10V |
| $Q_{rr}$ | Reverse Recovery Charge | — | 34 | 51 | nC | di/dt = 100A/µs ③ |
| $t_{rr}$ | Reverse Recovery Time | — | 35 | 53 | ns | $T_J$ = 125°C, $I_F$ = 18A, $V_R$=10V |
| $Q_{rr}$ | Reverse Recovery Charge | — | 35 | 53 | nC | di/dt = 100A/µs ③ |

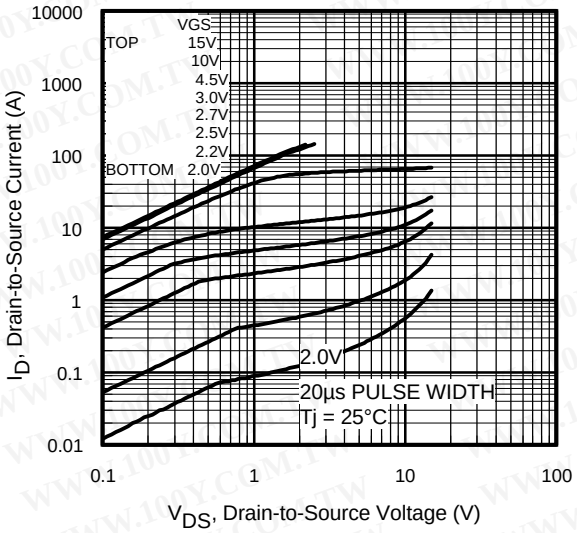



**Fig 1.** Typical Output Characteristics

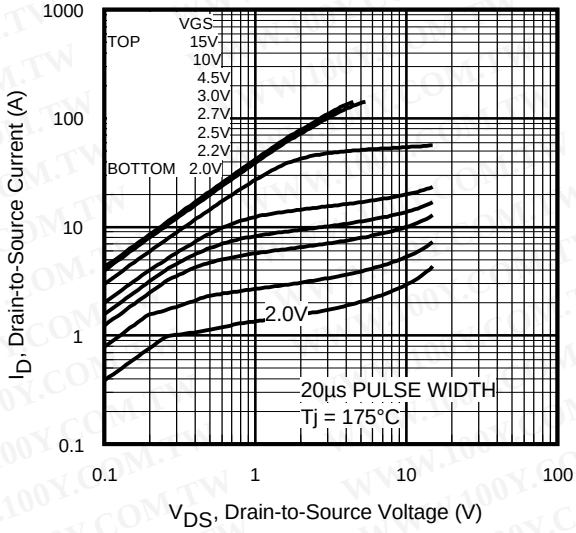



**Fig 2.** Typical Output Characteristics

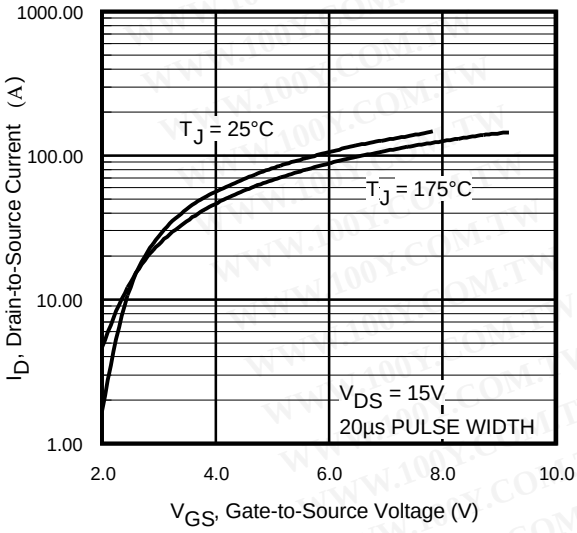



**Fig 3.** Typical Transfer Characteristics

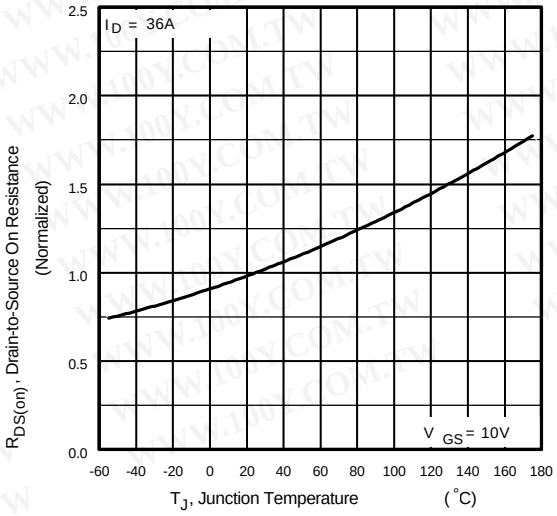



**Fig 4.** Normalized On-Resistance Vs. Temperature

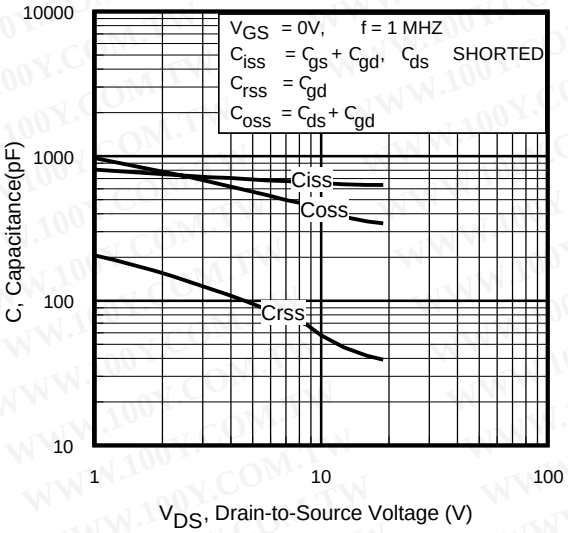



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

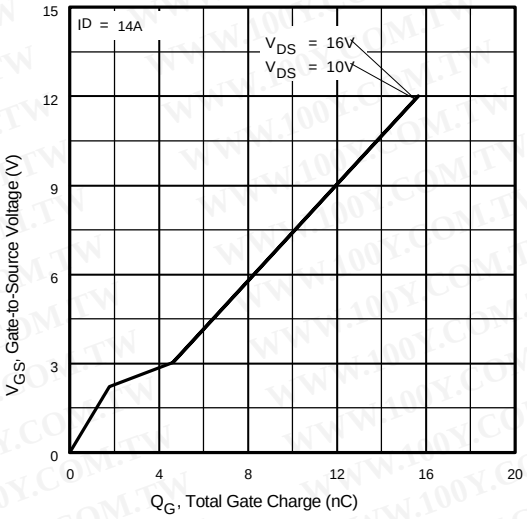



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

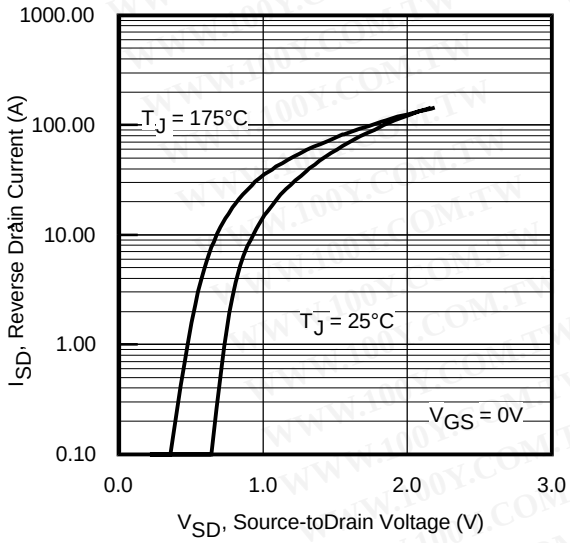



**Fig 7.** Typical Source-Drain Diode Forward Voltage

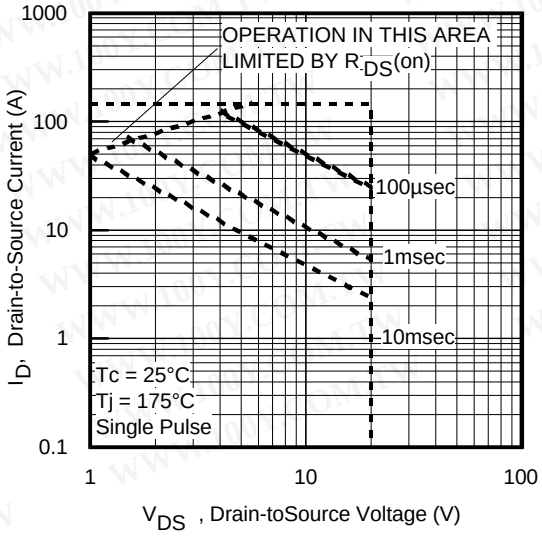



**Fig 8.** Maximum Safe Operating Area

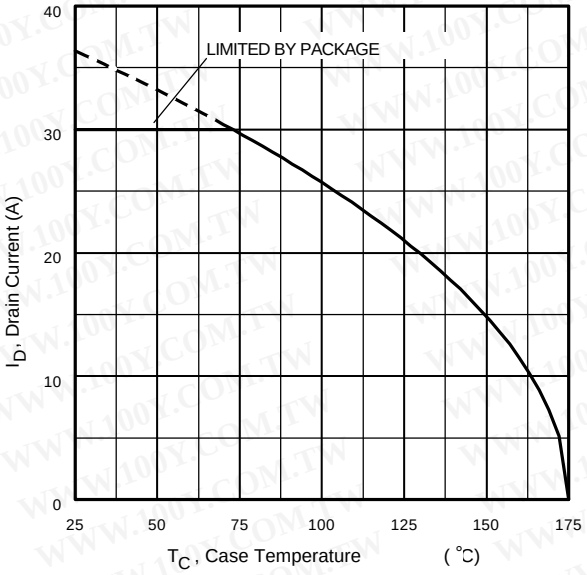



**Fig 9.** Maximum Drain Current Vs. Case Temperature

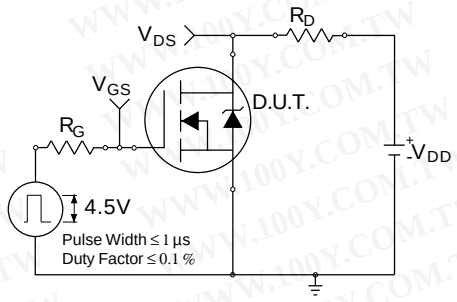



**Fig 10a.** Switching Time Test Circuit

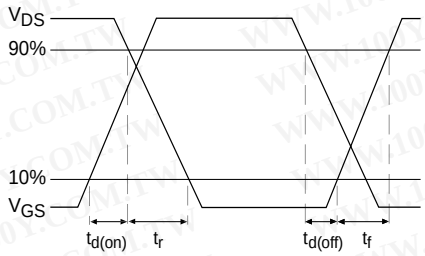



**Fig 10b.** Switching Time Waveforms

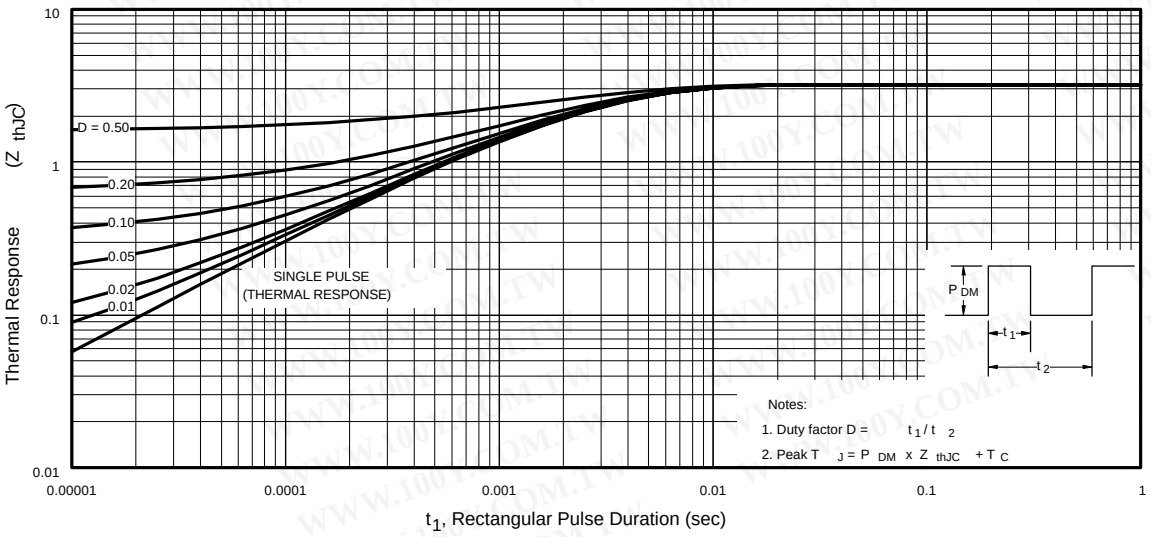



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

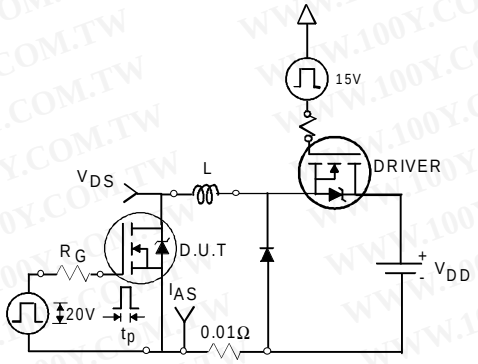



**Fig 12a.** Unclamped Inductive Test Circuit

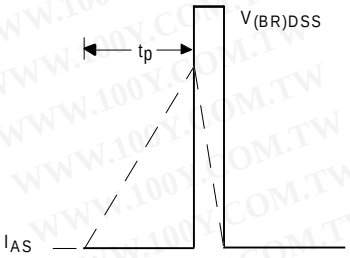



**Fig 12b.** Unclamped Inductive Waveforms

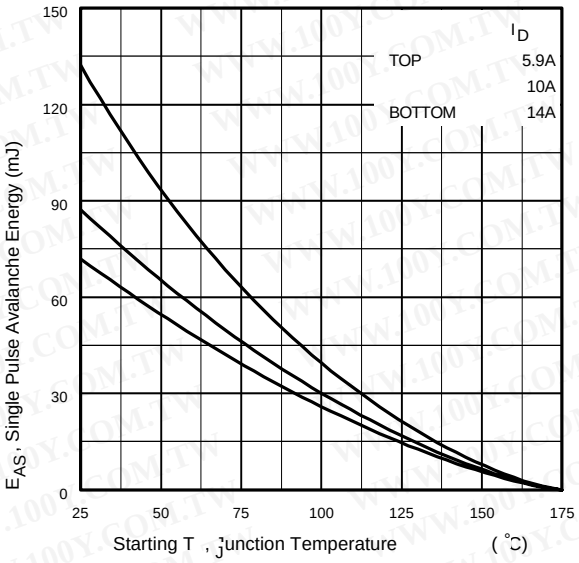



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

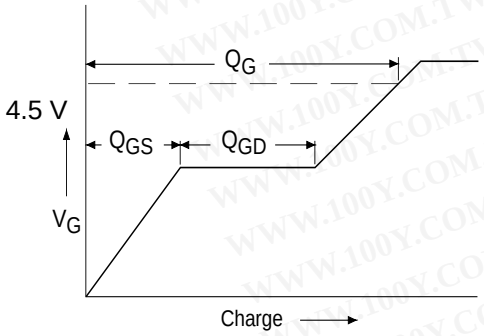



**Fig 13a.** Basic Gate Charge Waveform

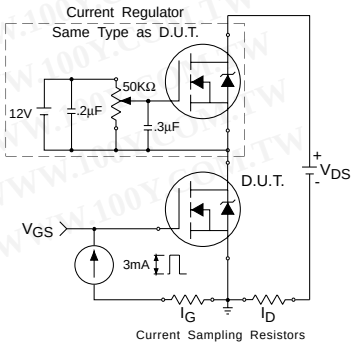
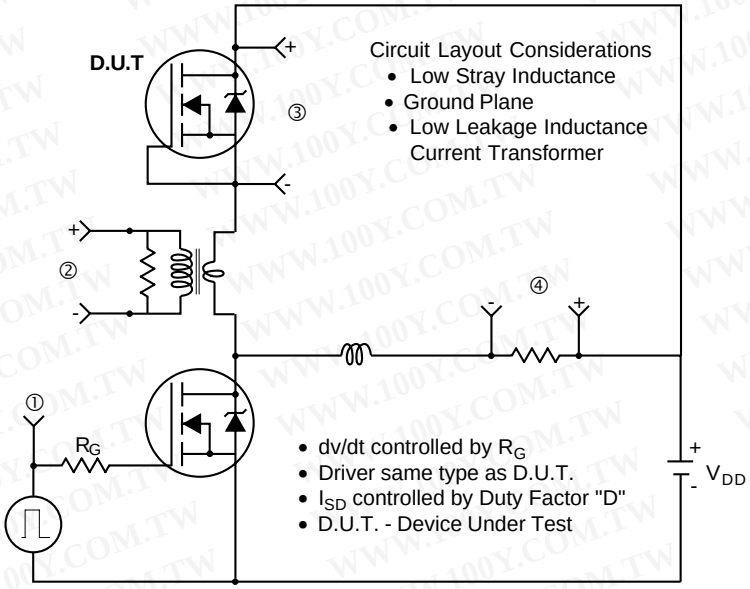
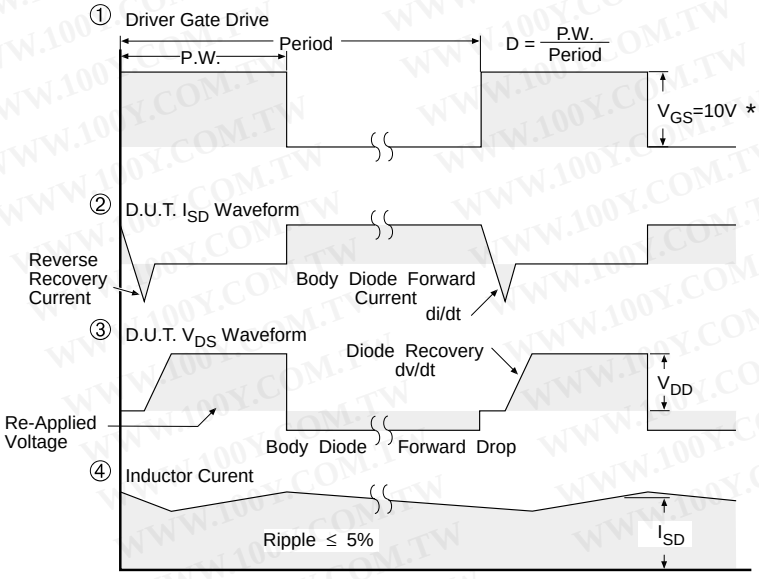



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



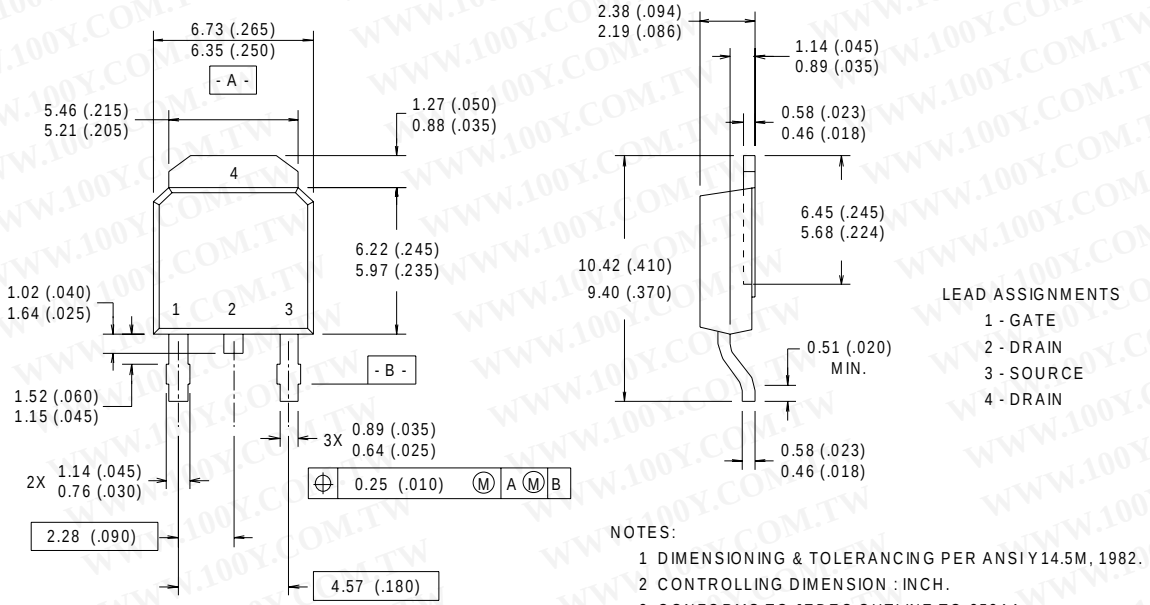




* $V_{GS}$ = 5V for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

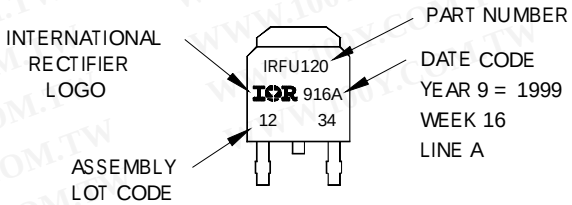



LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

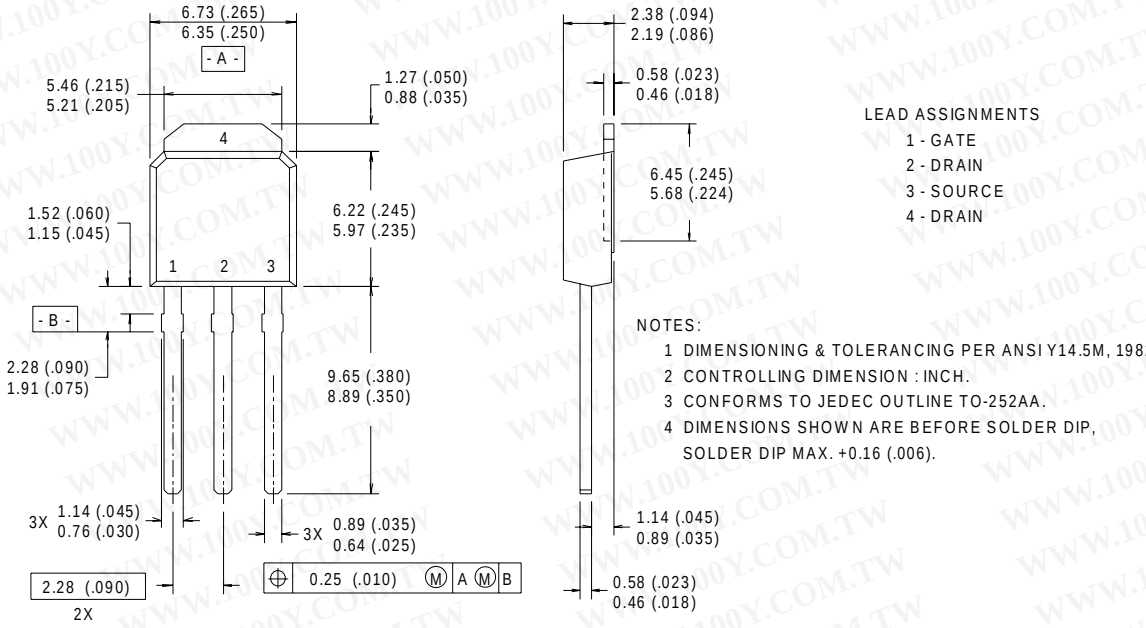
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

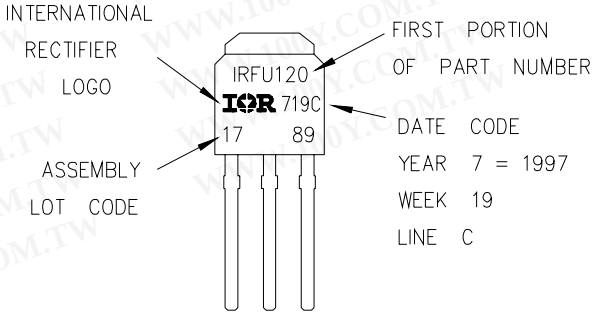



LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

## I-Pak (TO-251AA) Part Marking Information

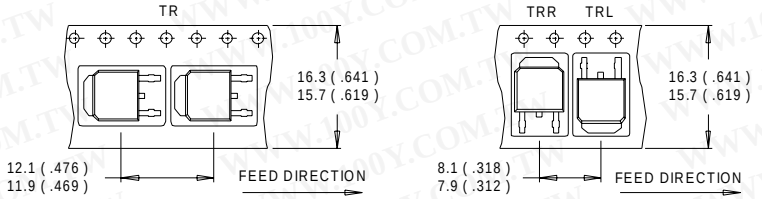
EXAMPLE: THIS IS AN IRFU120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



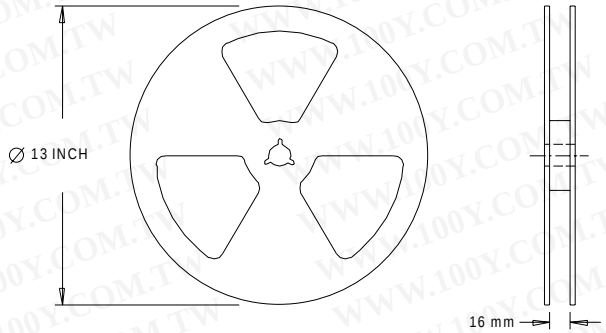
International
IOR Rectifier

## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)




NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.




NOTES :
1. OUTLINE CONFORMS TO EIA-481.

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J$ = 25°C, L = 0.69 mH
$R_G$ = 25Ω, $I_{AS}$ = 14A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ When mounted on 1" square PCB ( FR-4 or G-10 Material ). For recommended footprint and soldering techniques refer to application note #AN-994.

⑤ Calculated continuous current based on maximum allowable junction temperature; Package limitation current is 30A