

International **IR** Rectifier

SMPS MOSFET

PD - 94296A
 IRFR12N25D
 IRFU12N25D
 HEXFET® Power MOSFET

Applications

- High frequency DC-DC converters

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

V_{DSS}	$R_{DS(on)}$ max	I_D
250V	0.26 Ω	14A



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	14	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	9.7	
I_{DM}	Pulsed Drain Current ①	56	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	144	W
	Linear Derating Factor	0.96	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	9.3	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$
T_{STG}	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.04	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Notes ① through ⑤ are on page 10

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	250	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.29	—	$V/^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.26	Ω	$V_{GS} = 10V$, $I_D = 8.4A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V$, $V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

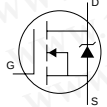
Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	6.8	—	—	S	$V_{DS} = 25V$, $I_D = 8.4A$
Q_g	Total Gate Charge	—	23	35	nC	$I_D = 8.4A$
Q_{gs}	Gate-to-Source Charge	—	5.8	8.7		$V_{DS} = 200V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	12	19		$V_{GS} = 10V$, ④
$t_{d(on)}$	Turn-On Delay Time	—	9.1	—	ns	$V_{DD} = 125V$
t_r	Rise Time	—	25	—		$I_D = 8.4A$
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	9.2	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	810	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	130	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	22	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	1100	—		$V_{GS} = 0V$, $V_{DS} = 1.0V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	50	—		$V_{GS} = 0V$, $V_{DS} = 200V$, $f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	130	—		$V_{GS} = 0V$, $V_{DS} = 0V$ to $200V$ ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	250	mJ
I_{AR}	Avalanche Current①	—	8.4	A
E_{AR}	Repetitive Avalanche Energy①	—	14	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	14	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	56		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}$, $I_S = 8.4A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	140	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 8.4A$
Q_{rr}	Reverse Recovery Charge	—	710	—	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

IRFR12N25D/IRFU12N25D

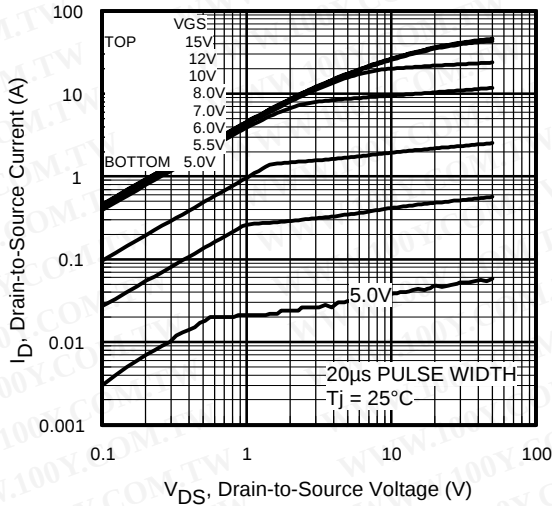


Fig 1. Typical Output Characteristics

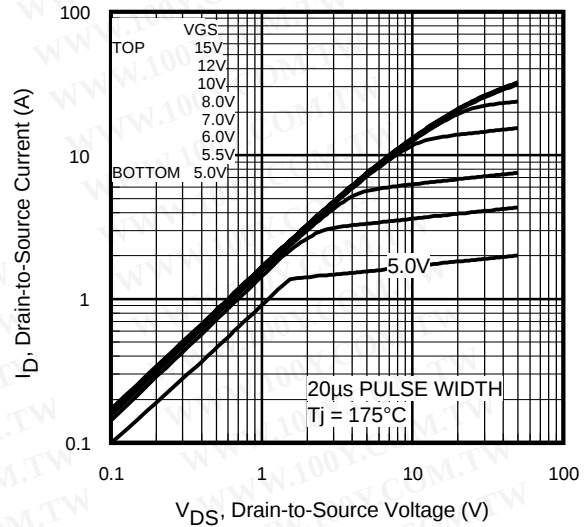


Fig 2. Typical Output Characteristics

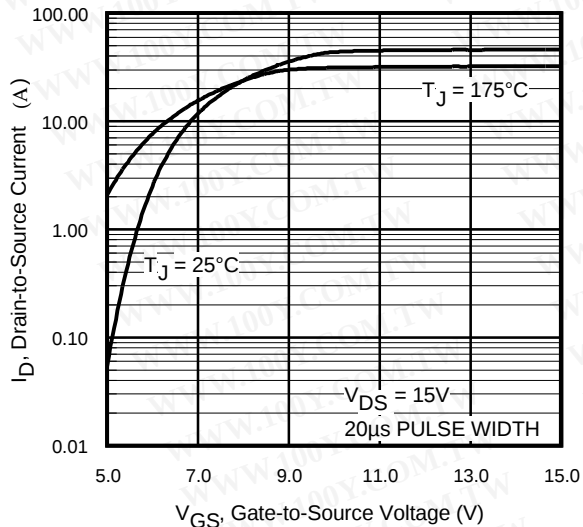


Fig 3. Typical Transfer Characteristics

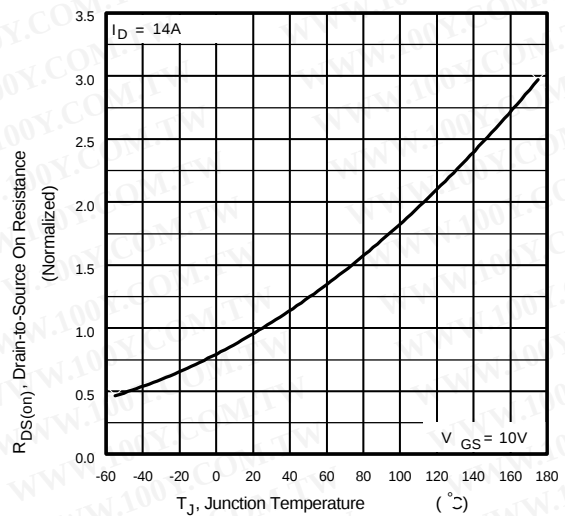


Fig 4. Normalized On-Resistance Vs. Temperature

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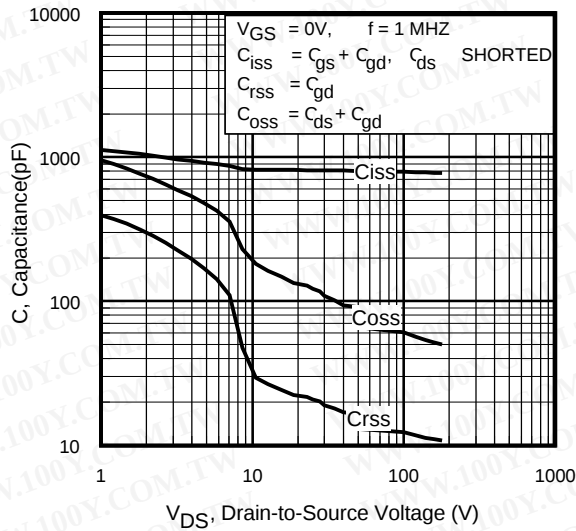


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

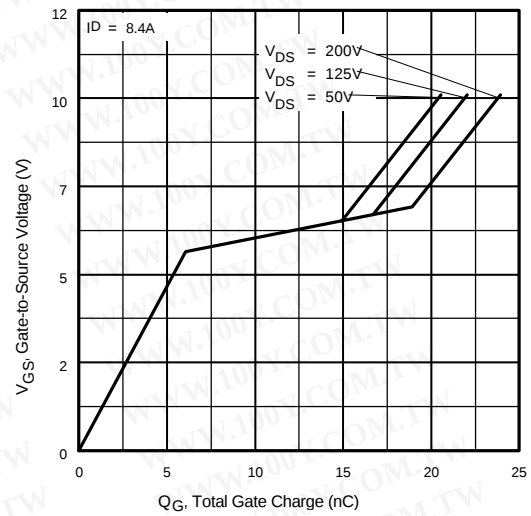


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

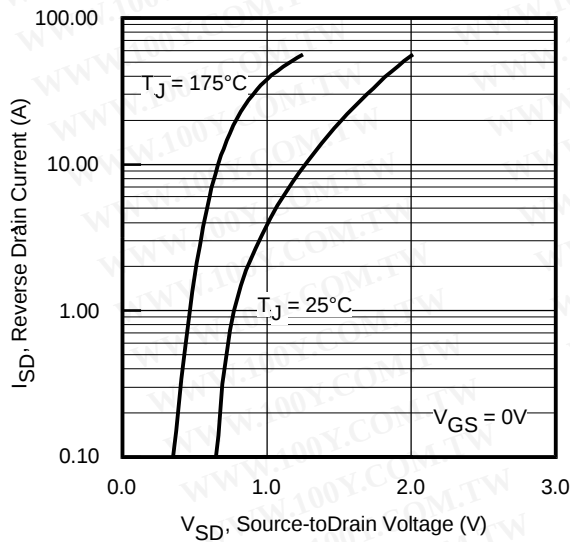


Fig 7. Typical Source-Drain Diode Forward Voltage

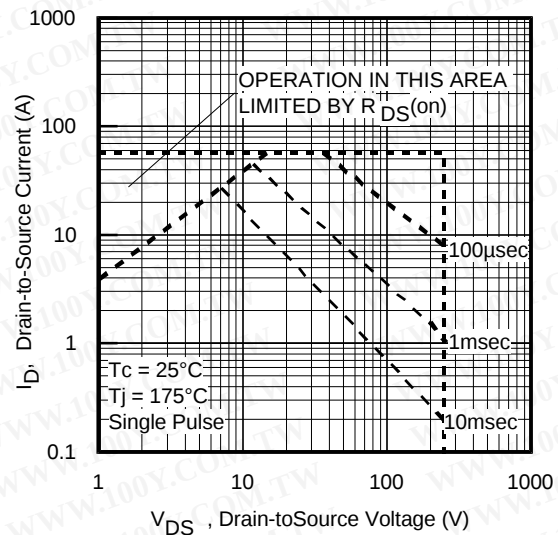


Fig 8. Maximum Safe Operating Area

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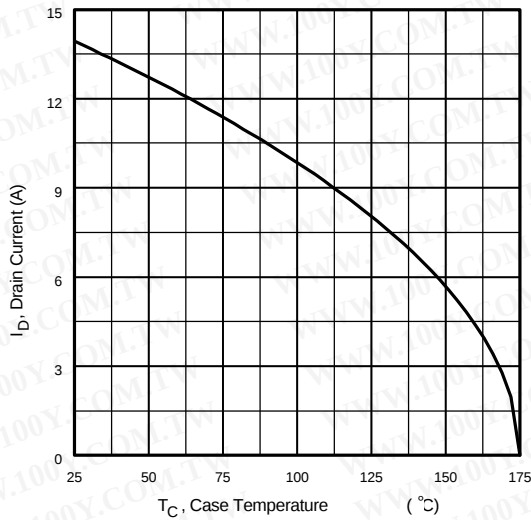


Fig 9. Maximum Drain Current Vs. Case Temperature

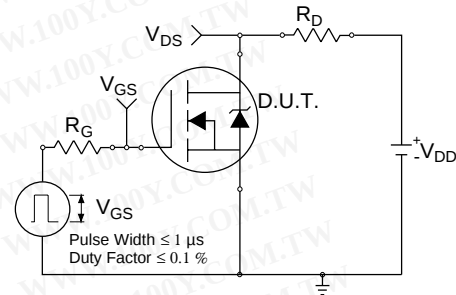


Fig 10a. Switching Time Test Circuit

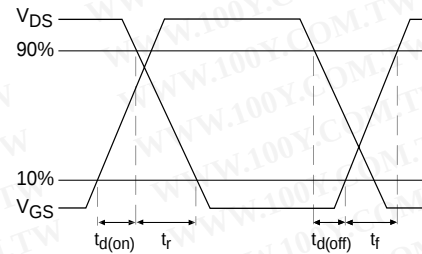


Fig 10b. Switching Time Waveforms

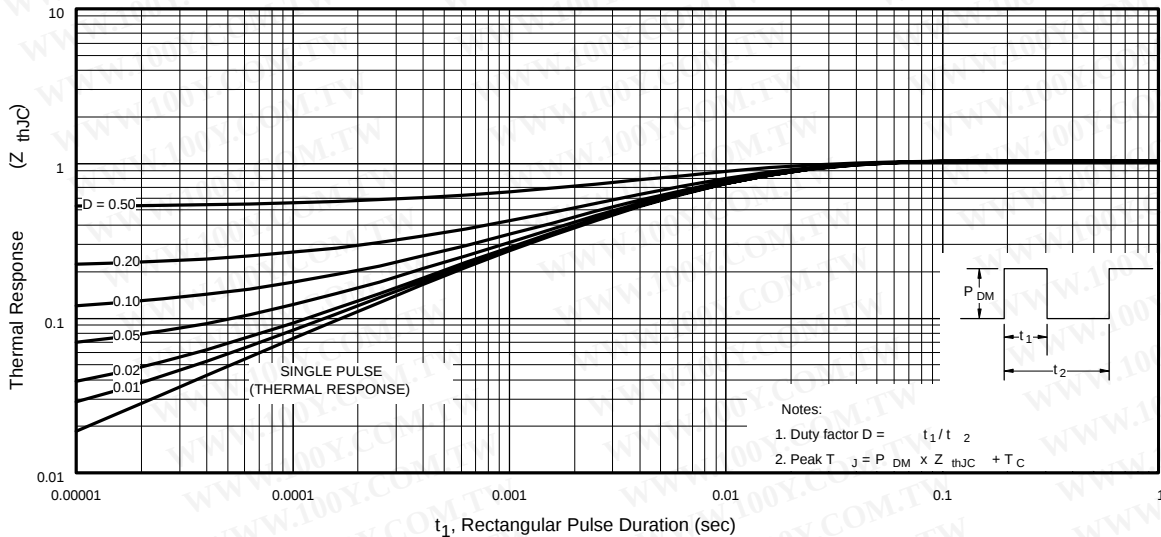


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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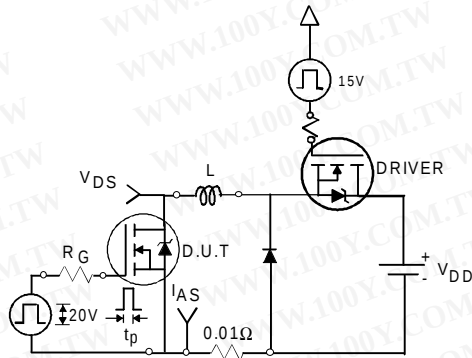


Fig 12a. Unclamped Inductive Test Circuit

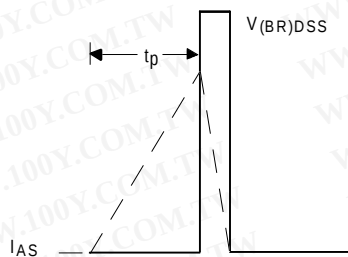


Fig 12b. Unclamped Inductive Waveforms

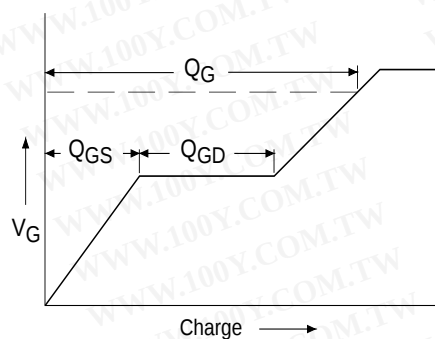


Fig 13a. Basic Gate Charge Waveform

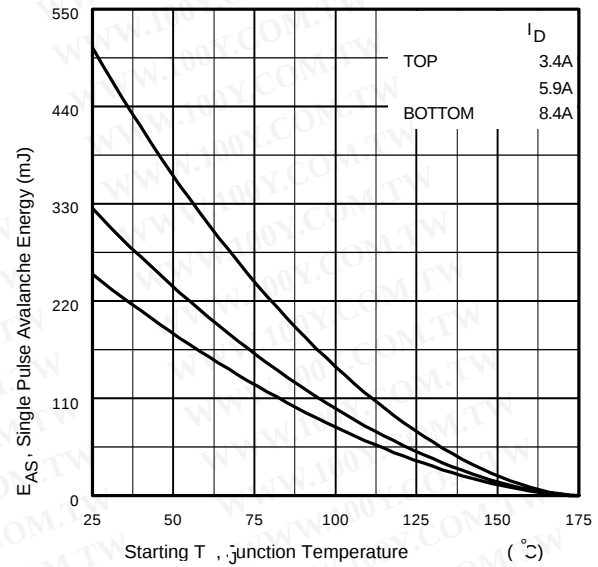


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

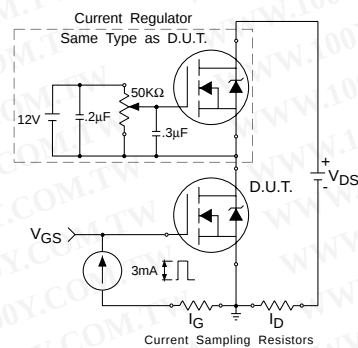
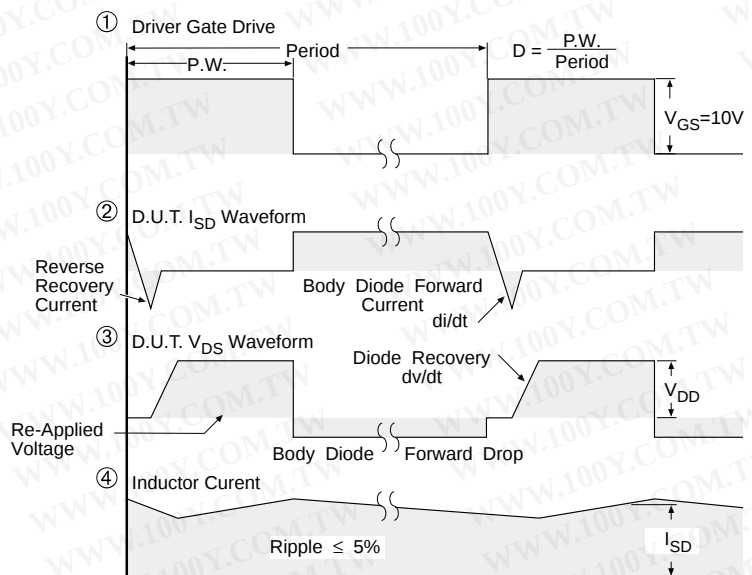
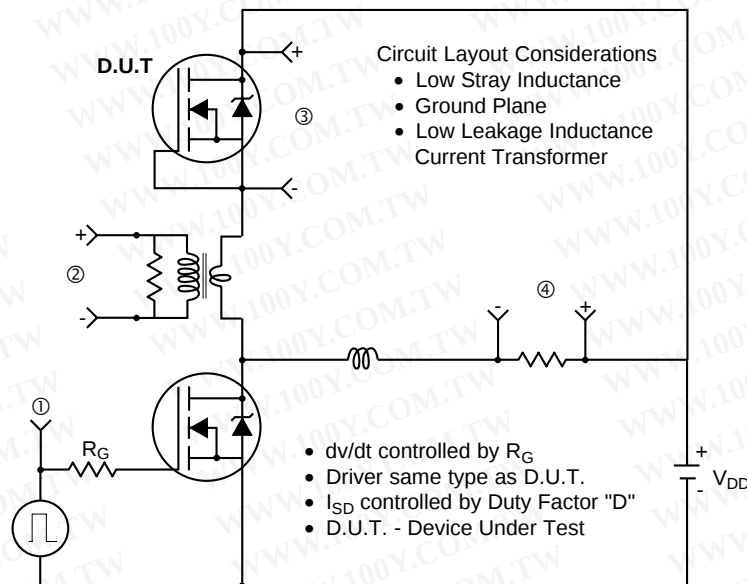


Fig 13b. Gate Charge Test Circuit

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Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

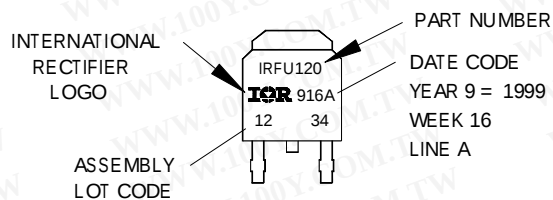
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Dimensions are shown in millimeters (inches)



- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,
SOLDER DIP MAX. +0.16 (.006).

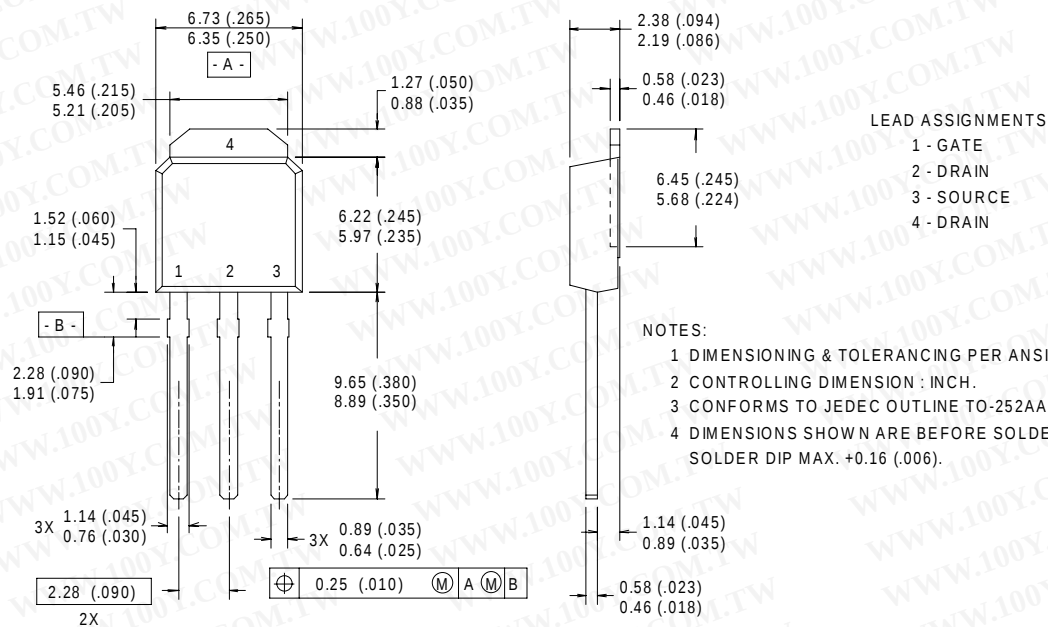
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



IRFR12N25D/IRFU12N25D

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

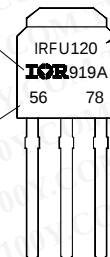


I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE



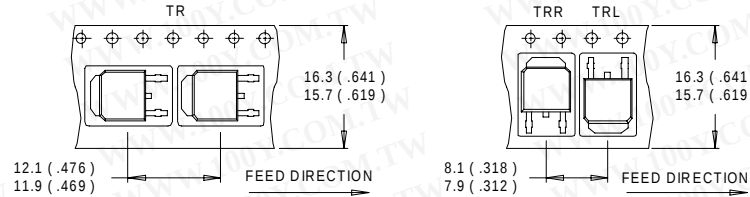
PART NUMBER
DATE CODE
YEAR 9 = 1999
WEEK 19
LINE A

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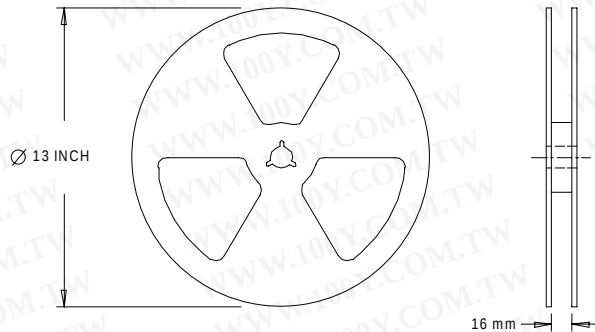
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D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
 - ② Starting $T_J = 25^\circ\text{C}$, $L = 7.1\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 8.4\text{A}$.
 - ③ $I_{SD} \leq 8.4\text{A}$, $di/dt \leq 150\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
 - ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
 - ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- * When mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Automotive [Q101] market.
 Qualification Standards can be found on IR's Web site.

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