

# FDY4000CZ

## Complementary N & P-Channel PowerTrench® MOSFET

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 0.7Ω at  $V_{GS} = 4.5V$ ,  $I_D = 600mA$
- Max  $r_{DS(on)}$  = 0.85Ω at  $V_{GS} = 2.5V$ ,  $I_D = 500mA$
- Max  $r_{DS(on)}$  = 1.25Ω at  $V_{GS} = 1.8V$ ,  $I_D = 150mA$

Q2: P-Channel

- Max  $r_{DS(on)}$  = 1.2Ω at  $V_{GS} = -4.5V$ ,  $I_D = -350mA$
- Max  $r_{DS(on)}$  = 1.6Ω at  $V_{GS} = -2.5V$ ,  $I_D = -300mA$
- Max  $r_{DS(on)}$  = 2.7Ω at  $V_{GS} = -1.8V$ ,  $I_D = -150mA$
- ESD protection diode (note 3)
- RoHS Compliant

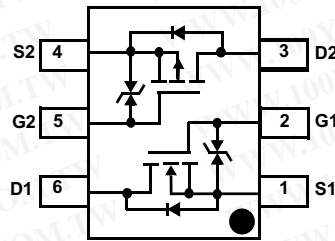
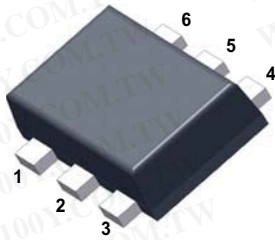


### General Description

This Complementary N & P-Channel MOSFET has been designed using Fairchild Semiconductor's advanced PowerTrench® process to optimize the  $r_{DS(on)}$  @  $V_{GS} = 2.5V$  and specify the  $r_{DS(on)}$  @  $V_{GS} = 1.8V$ .

### Applications

- Level shifting
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers



### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	20	-20	V
$V_{GS}$	Gate to Source Voltage	±12	±8	V
$I_D$	Drain Current -Continuous	600	-350	mA
	-Pulsed	1000	-1000	
$P_D$	Power Dissipation (Steady State)	(Note 1a)	625	mW
		(Note 1b)	446	
$T_J, T_{STG}$	Operating and Storage Jaunting Temperature Range	-55 to 150		°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	200	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	280	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
E	FDY4000CZ	SC89-6	7"	8mm	3000units

### Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	Q1	20			V
		$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	Q2	-20			
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1		15		mV/ $^\circ\text{C}$
		$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$	Q2		-15		
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$	Q1			1	$\mu\text{A}$
		$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$	Q2			-3	
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$	Q1			$\pm 10$	$\mu\text{A}$
		$V_{GS} = \pm 4.5\text{V}, V_{DS} = 0\text{V}$	Q1			$\pm 1$	
		$V_{GS} = \pm 8\text{V}, V_{DS} = 0\text{V}$	Q2			$\pm 10$	

### On Characteristics (note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	Q1	0.6	1.0	1.5	V
		$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	Q2	-0.6	-1.0	-1.5	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1		-3		mV/ $^\circ\text{C}$
		$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$	Q2		3		
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{V}, I_D = 600\text{mA}$	Q1		0.30	0.70	$\Omega$
		$V_{GS} = 2.5\text{V}, I_D = 500\text{mA}$			0.40	0.85	
		$V_{GS} = 1.8\text{V}, I_D = 150\text{mA}$			0.80	1.25	
		$V_{GS} = 4.5\text{V}, I_D = 600\text{mA}, T_J = 125^\circ\text{C}$		0.35	1.00		
		$V_{GS} = -4.5\text{V}, I_D = -350\text{mA}$	Q2		0.5	1.2	
		$V_{GS} = -2.5\text{V}, I_D = -300\text{mA}$			0.8	1.6	
$V_{GS} = -1.8\text{V}, I_D = -150\text{mA}$		1.3		2.7			
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 600\text{mA}$	Q1		1.8		S
		$V_{DS} = -5\text{V}, I_D = -350\text{mA}$	Q2		1		

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1		60		pF
			Q2		100		
$C_{oss}$	Output Capacitance	Q2	Q1		20		pF
			Q2		30		
$C_{rss}$	Reverse Transfer Capacitance	$V_{DS} = -10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1		10		pF
			Q2		15		

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 10\text{V}, I_D = 1\text{A},$ $V_{GS} = 4.5\text{V}, R_g = 6\Omega$	Q1		6	12	ns
			Q2		6	12	
$t_r$	Rise Time	Q1 $V_{DD} = 10\text{V}, I_D = 1\text{A},$ $V_{GS} = 4.5\text{V}, R_g = 6\Omega$	Q1		8	16	ns
			Q2		13	23	
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -10\text{V}, I_D = -0.5\text{A},$ $V_{GS} = -4.5\text{V}, R_g = 6\Omega$	Q1		8	16	ns
			Q2		8	16	
$t_f$	Fall Time	Q2 $V_{DD} = -10\text{V}, I_D = -0.5\text{A},$ $V_{GS} = -4.5\text{V}, R_g = 6\Omega$	Q1		2.4	4.8	ns
			Q2		1	2	
$Q_g$	Total Gate Charge	Q1 $V_{DS} = 10\text{V}, I_D = 600\text{mA}, V_{GS} = 4.5\text{V}$	Q1		0.8	1.1	nC
			Q2		1.0	1.4	
$Q_{gs}$	Gate to Source Gate Charge	Q1 $V_{DS} = 10\text{V}, I_D = 600\text{mA}, V_{GS} = 4.5\text{V}$	Q1		0.16		nC
			Q2		0.2		
$Q_{gd}$	Gate to Drain "Miller" Charge	Q2 $V_{DS} = -10\text{V}, I_D = -350\text{mA}, V_{GS} = -4.5\text{V}$	Q1		0.26		nC
			Q2		0.3		

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

**Drain-Source Diode Characteristics**

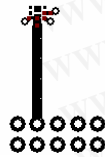
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 150\text{mA}$ (Note 2) $V_{GS} = 0\text{V}, I_S = -150\text{mA}$ (Note 2)	Q1 Q2		0.7 -0.8	1.2 -1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 600\text{mA}, di/dt = 100\text{A}/\mu\text{s}$	Q1 Q2		8 11		ns
$Q_{rr}$	Reverse Recovery Charge	$I_F = -350\text{mA}, di/dt = 100\text{A}/\mu\text{s}$	Q1 Q2		1 2		nC

**Notes:**

**1:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a)  $200^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $280^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

Scale 1:1 on letter size paper

**2:** Pulse Test : Pulse Width < 300us, Duty Cycle < 2.0%

**3:** The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

### Typical Characteristics Q1 (N-Channel)

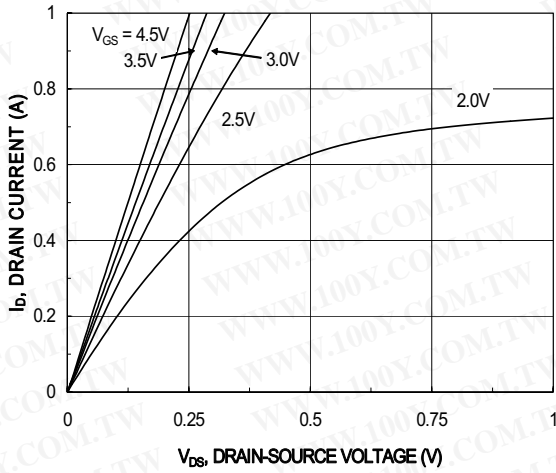


Figure 1. On-Region Characteristics

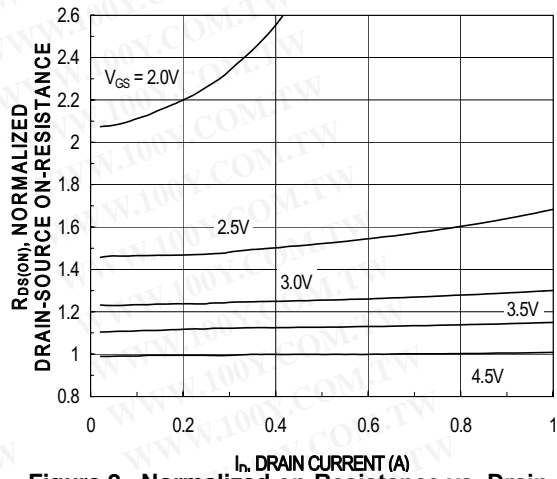


Figure 2. Normalized on-Resistance vs. Drain Current and Gate Voltage

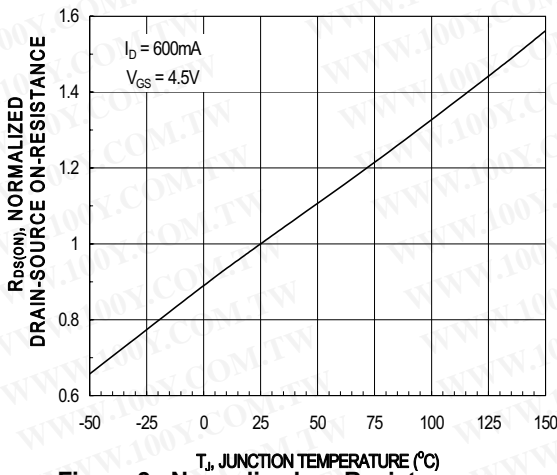


Figure 3. Normalized on-Resistance vs. Temperature

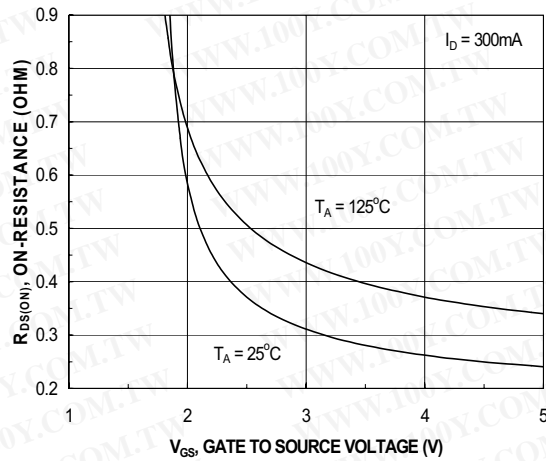


Figure 4. On-Resistance vs. Gate-to-Source Voltage

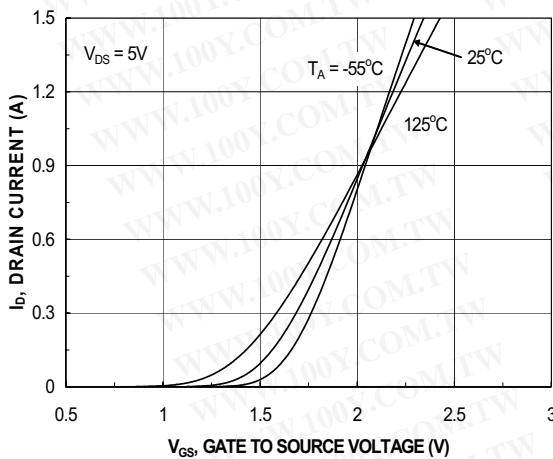


Figure 5. Transfer Characteristics

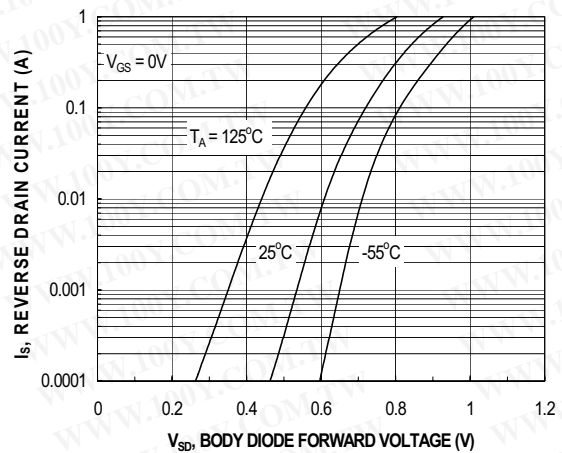


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current and Temperature

### Typical Characteristics Q1 (N-Channel)

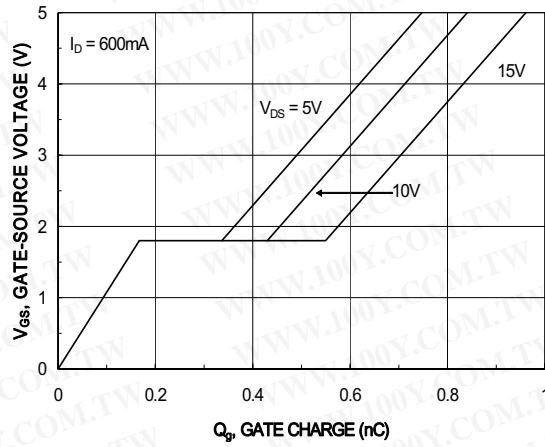


Figure 7. Gate Charge Characteristics

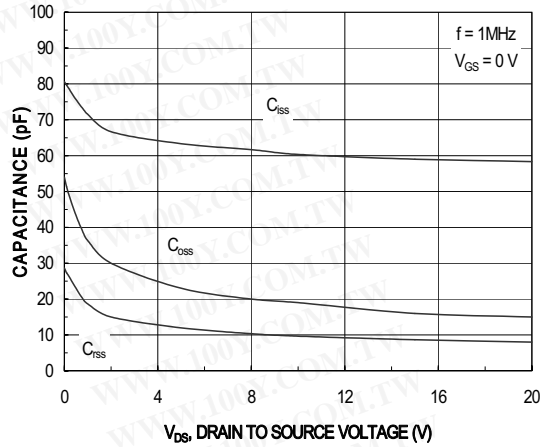


Figure 8. Capacitance vs. Drain to source voltage

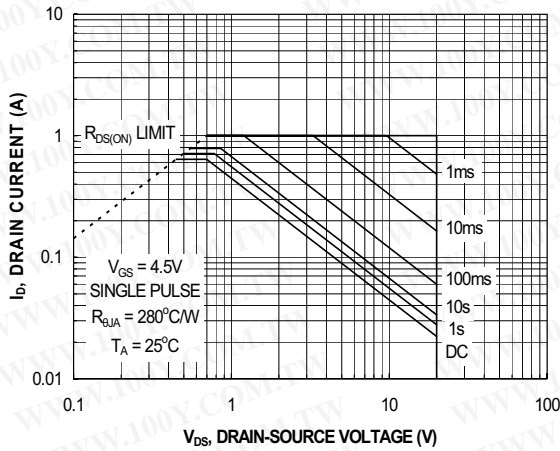


Figure 9. Maximum Safe Operating Area

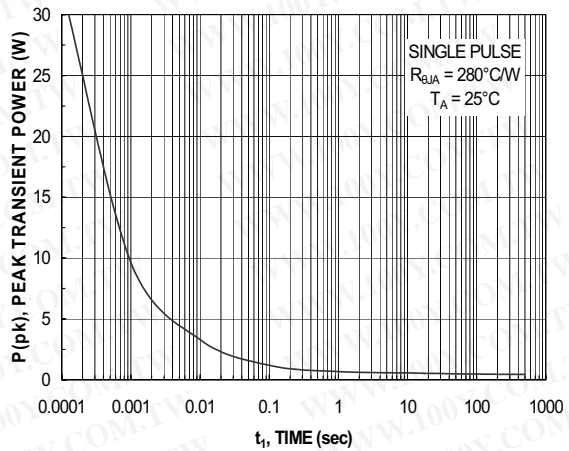


Figure 10. Single Pulse Maximum Power Dissipation

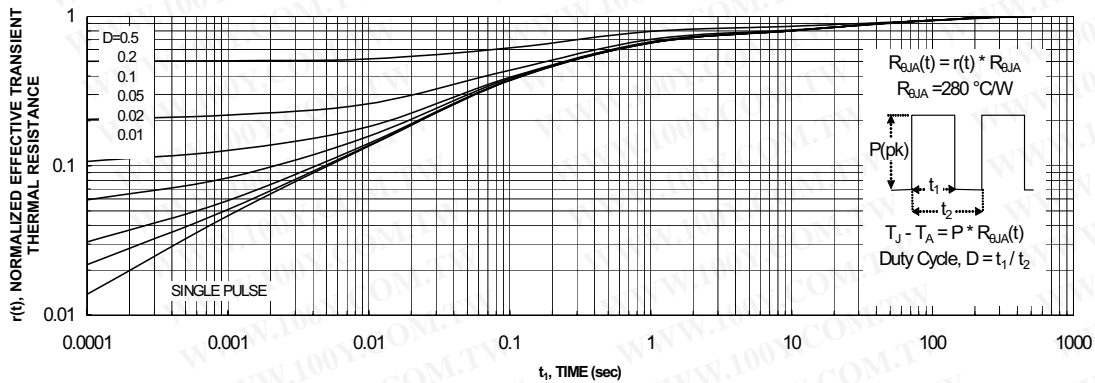


Figure 11. Transient Thermal Response Curve  
Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.

### Typical Characteristics Q2 (P-Channel)

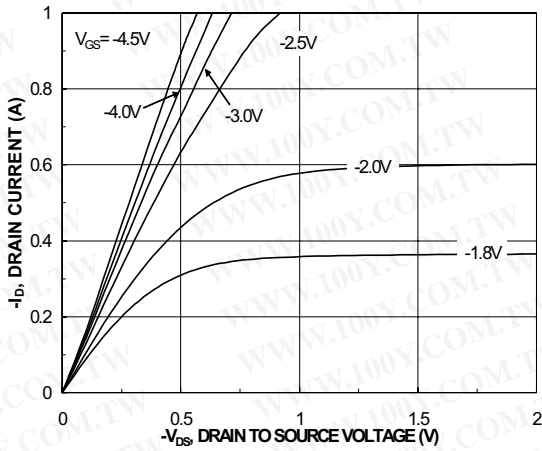


Figure 12. On-Region Characteristics

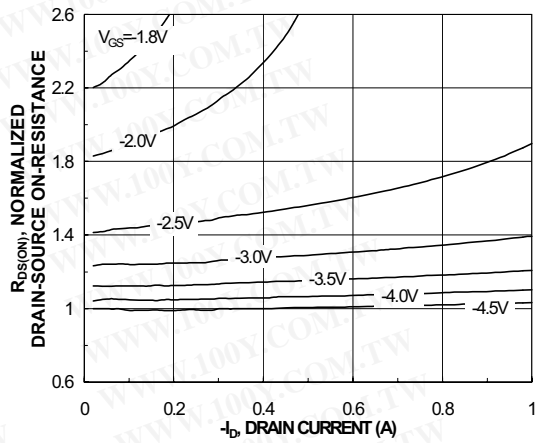


Figure 13. Normalized on-Resistance vs. Drain Current and Gate Voltage

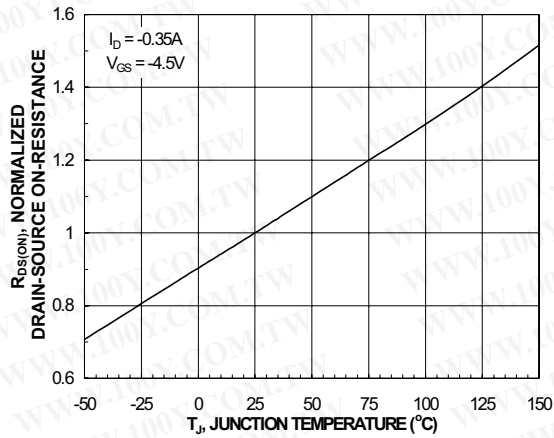


Figure 14. Normalized on-Resistance vs. Temperature

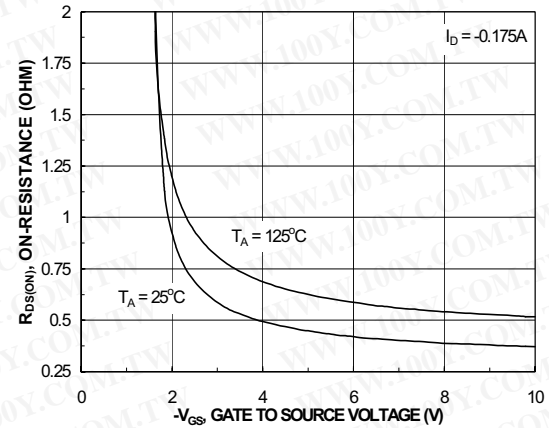


Figure 15. On-Resistance vs. Gate-to-Source Voltage

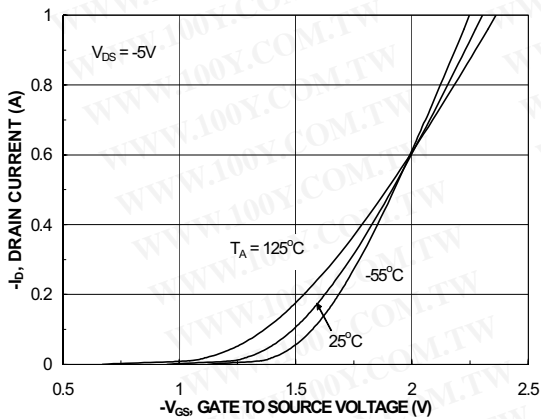


Figure 16. Transfer Characteristics

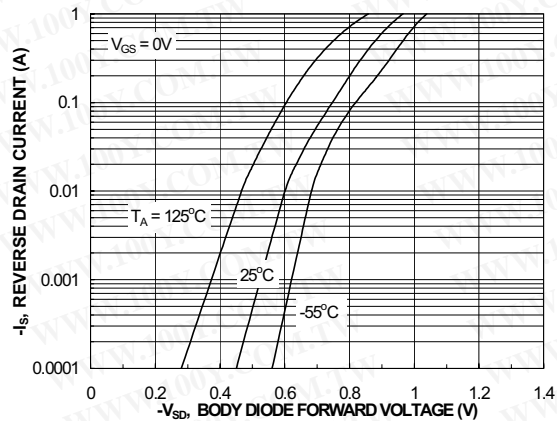
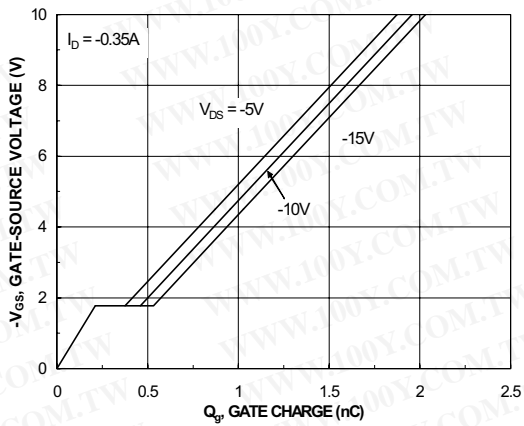
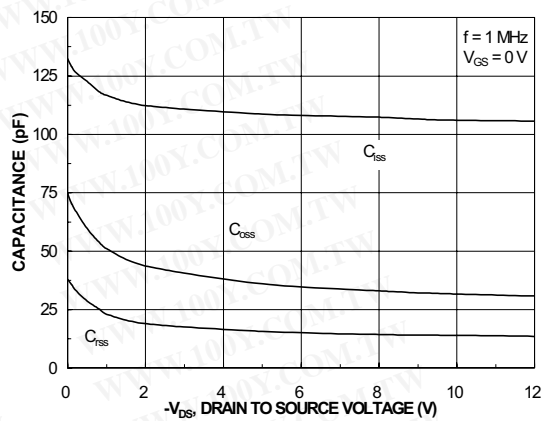


Figure 17. Source to Drain Diode Forward Voltage vs. Source Current and Temperature

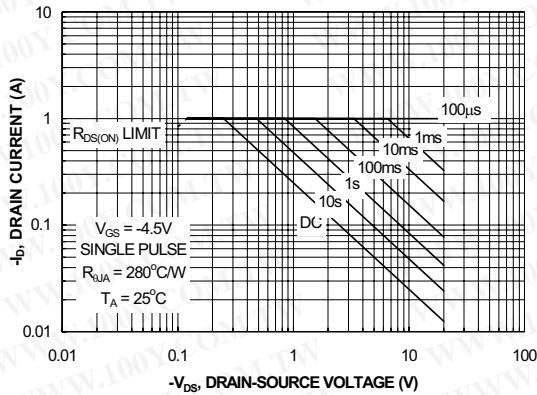
### Typical Characteristics Q2 (P-Channel)



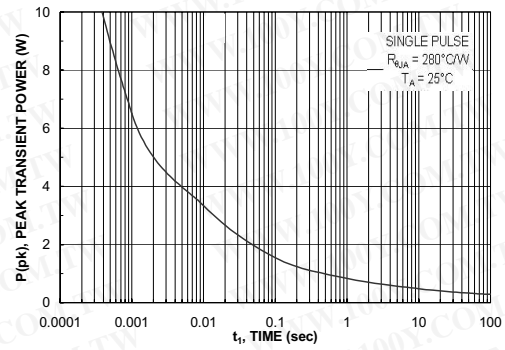
**Figure 18. Gate Charge Characteristics**



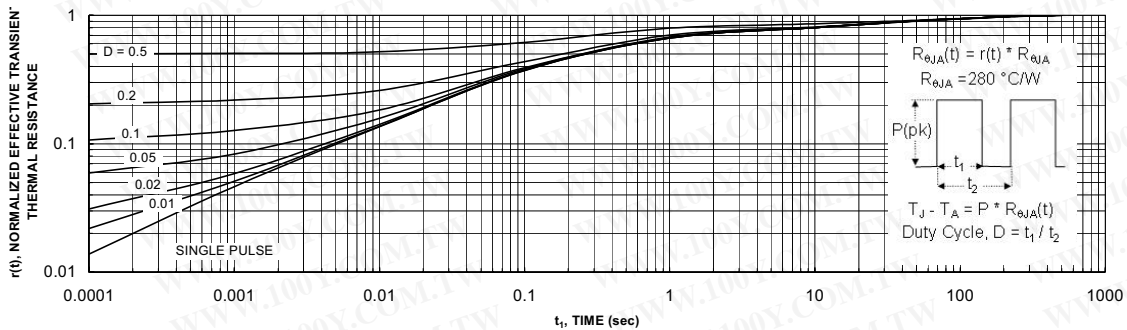
**Figure 19. Capacitance vs. Drain to source voltage**



**Figure 20. Maximum Safe Operating Area**

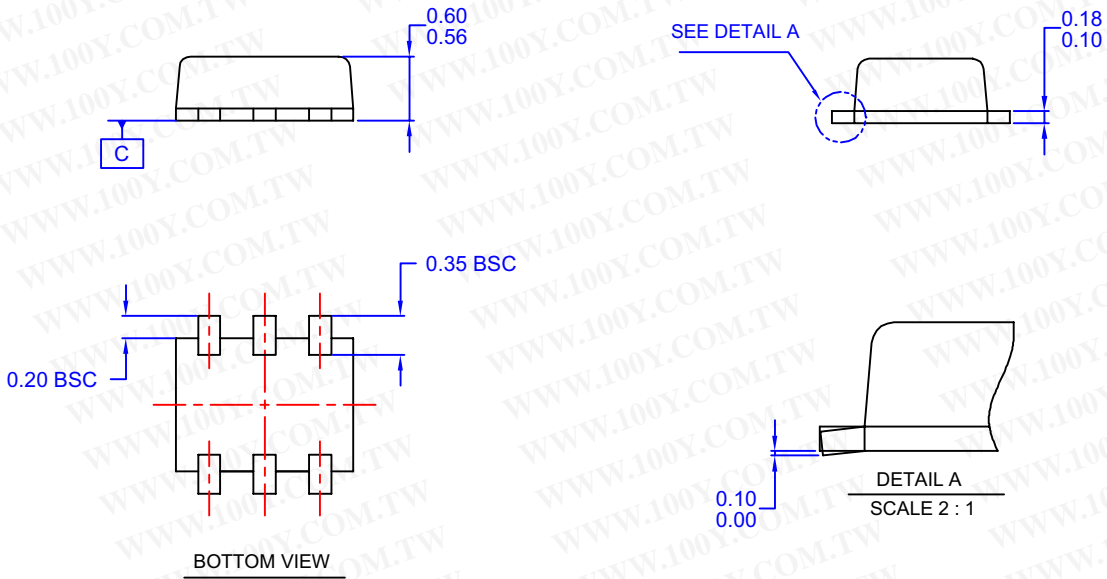
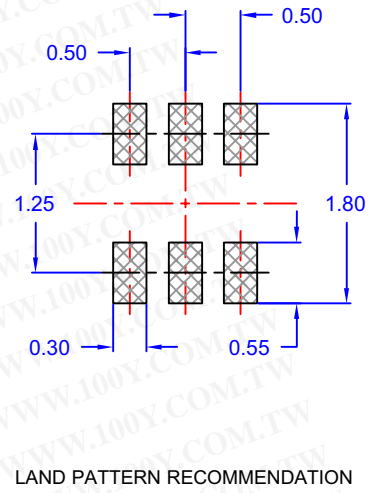
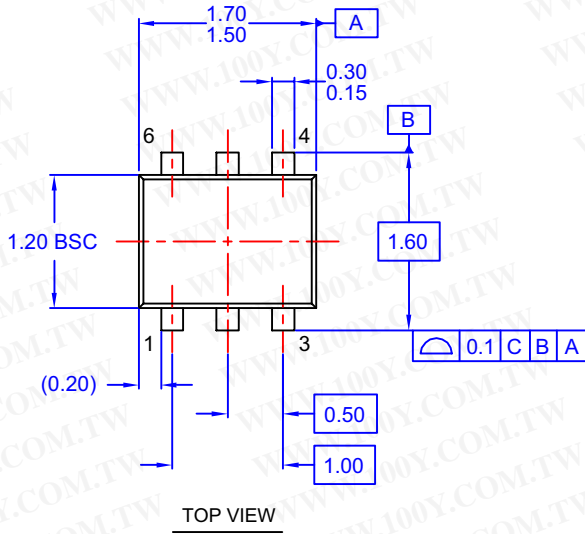


**Figure 21. Single Pulse Maximum Power Dissipation**



**Figure 22. Transient Thermal Response Curve**  
 Thermal characterization performed using the conditions described in Note 1b.  
 Transient thermal response will change depending on the circuit board design.

### Dimensional Outline and Pad Layout




**NOTES:**

- A) THIS PACKAGE CONFORMS TO EIAJ SC89 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

MAD06ArevA

**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™	FPS™	PowerTrench®	The Power Franchise®
Auto-SPM™	F-PFS™	PowerXS™	the <b>power</b> ®
Build it Now™	FRFET®	Programmable Active Droop™	franchise
CorePLUS™	Global Power ResourceSM	QFET®	TinyBoost™
CorePOWER™	Green FPS™	QS™	TinyBuck™
CROSSVOLT™	Green FPS™ e-Series™	Quiet Series™	TinyCalc™
CTL™	Gmax™	RapidConfigure™	TinyLogic®
Current Transfer Logic™	GTO™	 ™	TINYOPTO™
EcoSPARK®	IntelliMAX™	Saving our world, 1mW /W /kW at a time™	TinyPower™
EfficientMax™	ISOPLANAR™	SmartMax™	TinyPWM™
EZSWITCH™*	MegaBuck™	SMART START™	TinyWire™
 ™	MICROCOUPLER™	SPM®	TriFault Detect™
 ™	MicroFET™	STEALTH™	TRUECURRENT™*
Fairchild®	MicroPak™	SuperFET™	 ™
Fairchild Semiconductor®	MillerDrive™	SuperSOT™-3	UHC®
FACT Quiet Series™	MotionMax™	SuperSOT™-6	Ultra FRFET™
FACT®	Motion-SPM™	SuperSOT™-8	UniFET™
FAST®	OPTOLOGIC®	SupreMOS™	VCX™
FastvCore™	OPTOPLANAR®	SyncFET™	VisualMax™
FETBench™	 ™	Sync-Lock™	XS™
FlashWriter®*	PDP SPM™	 ™*	
	Power-SPM™		

\*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 141