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FDS9933A

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Dual P-Channel 2.5V Specified PowerTrench™ MOSFET

General Description

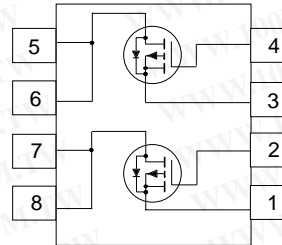
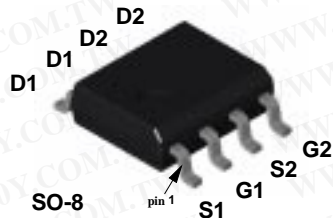
These P-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- Load switch
- DC/DC converter
- Motor drives

Features

- -3.8 A, -20 V. $R_{DS(on)} = 0.075 \Omega @ V_{GS} = -4.5 V$
 $R_{DS(on)} = 0.105 \Omega @ V_{GS} = -2.5 V$.
- Low gate charge (7nC typical).
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(on)}$.
- High power and current handling capability.



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	FDS9933A	Units
V _{DSS}	Drain-Source Voltage	-20	V
V _{GSS}	Gate-Source Voltage	± 8	V
I _D	Drain Current - Continuous (Note 1a)	-3.8	A
	- Pulsed	-20	
P _D	Power Dissipation for Dual Operation	2.0	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1.0	
	(Note 1c)	0.9	
T _J , T _{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS9933A	FDS9933A	13"	12mm	2500 units

DMOS Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		-16		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-0.8	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		2.5		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -3.8\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -3.8\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = -2.5\text{ V}, I_D = -3.3\text{ A}$		0.058 0.086 0.084	0.075 0.12 0.105	Ω Ω Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5.0\text{ V}$	-10			A
g_{FS}	Forward Transconductance	$V_{DS} = -4.5\text{ V}, I_D = -3.8\text{ A}$		10		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		600		pF
C_{oss}	Output Capacitance			175		pF
C_{riss}	Reverse Transfer Capacitance			80		pF

Switching Characteristics (Note 2)

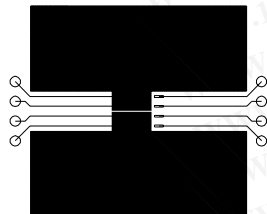
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -5\text{ V}, I_D = -0.5\text{ A}$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6.0\ \Omega$		6	12	ns
t_r	Turn-On Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			31	50	ns
t_f	Turn-Off Fall Time			28	42	ns
Q_g	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -3.8\text{ A}$ $V_{GS} = -4.5\text{ V}$		7	10	nC
Q_{gs}	Gate-Source Charge			1.3		nC
Q_{gd}	Gate-Drain Charge			2		nC

Drain-Source Diode Characteristics and Maximum Ratings

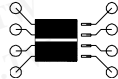
I_S	Maximum Continuous Drain-Source Diode Forward Current			-1.3	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)		-0.75	-1.2	V

Notes:

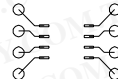
- 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz. copper.



b) 125°C/W when mounted on a 0.02 in^2 pad of 2 oz. copper.



c) 135°C/W when mounted on a 0.003 in^2 pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

- 2: Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics (continued)

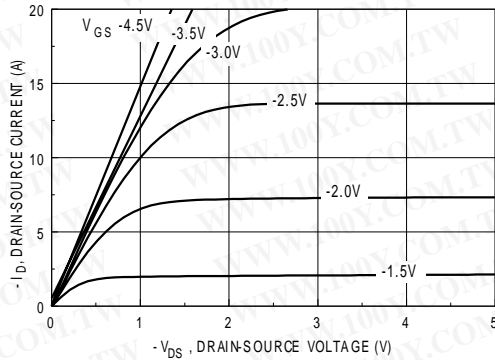


Figure 1. On-Region Characteristics.

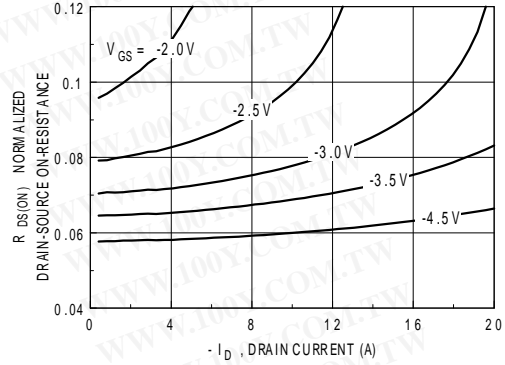


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

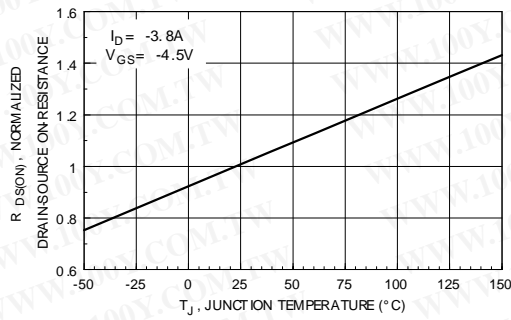


Figure 3. On-Resistance Variation with Temperature.

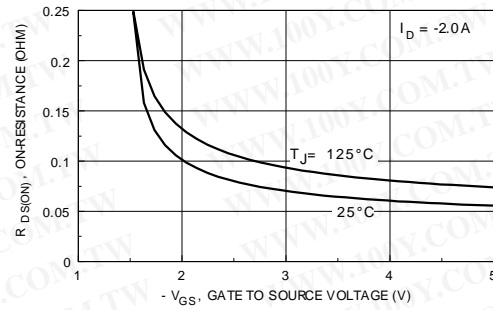


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

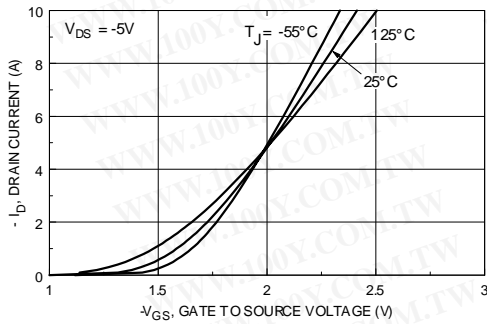


Figure 5. Transfer Characteristics.

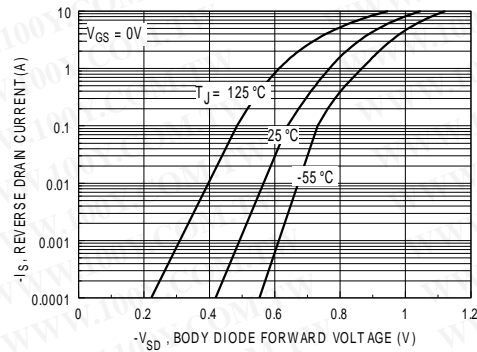


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

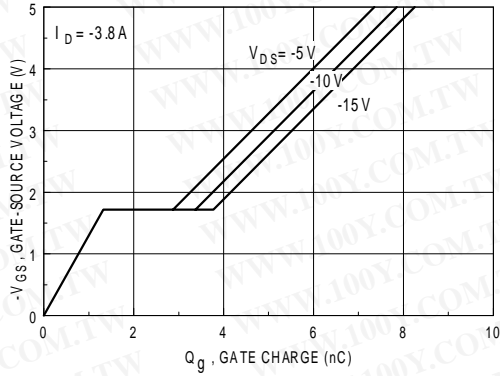


Figure 7. Gate Charge Characteristics.

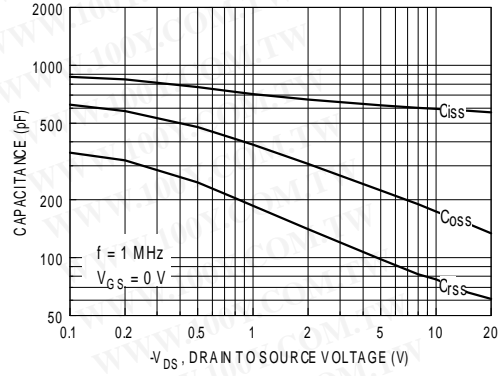


Figure 8. Capacitance Characteristics.

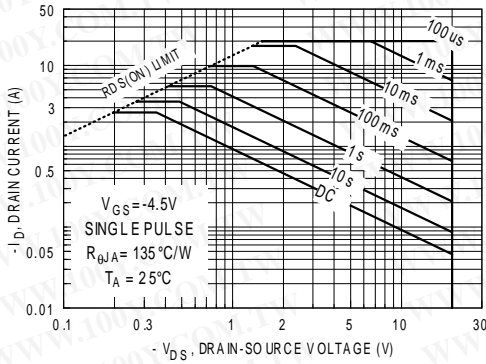


Figure 9. Maximum Safe Operating Area.

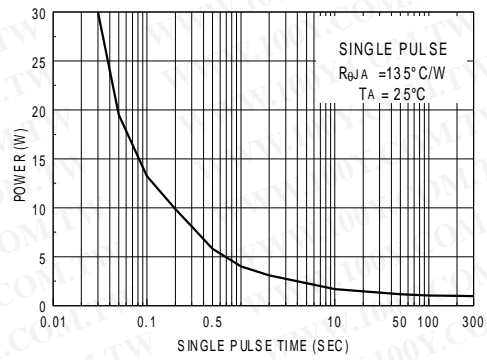


Figure 10. Single Pulse Maximum Power Dissipation.

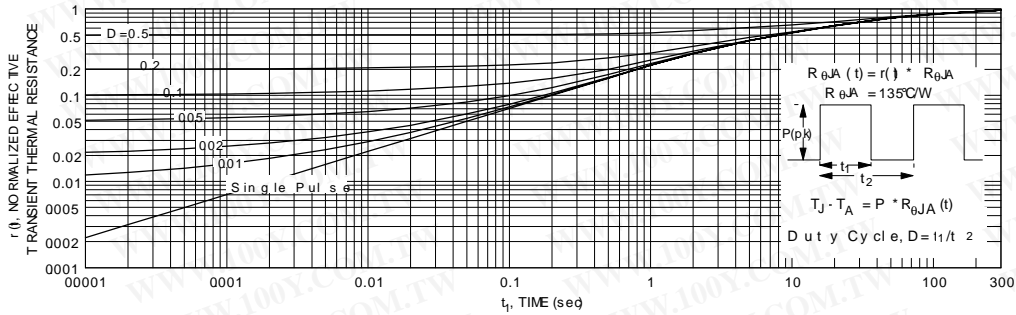


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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