

# FDS6612A

## Single N-Channel, Logic-Level, PowerTrench® MOSFET

### General Description

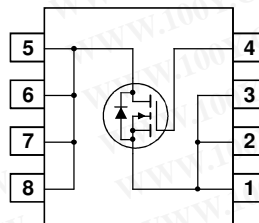
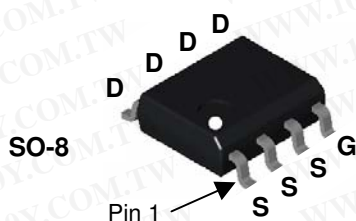
This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.



### Features

- 8.4 A, 30 V.  $R_{DS(ON)} = 22\text{ m}\Omega @ V_{GS} = 10\text{ V}$   
 $R_{DS(ON)} = 30\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	30	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	8.4	A
	– Pulsed	40	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.0	
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 3)	24	mJ
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	–55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1b)	125	
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	25	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6612A	FDS6612A	13"	12mm	2500 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		26		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			1 10	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-4.4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 8.4\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 7.2\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 8.4\text{ A}, T_J = 125^\circ\text{C}$		19 24 25	22 30 37	m $\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 8.4\text{ A}$		30		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		560		pF
$C_{oss}$	Output Capacitance			140		pF
$C_{rss}$	Reverse Transfer Capacitance			55		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		2.5		$\Omega$

### Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		7	14	ns
$t_r$	Turn-On Rise Time			5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			22	35	ns
$t_f$	Turn-Off Fall Time			3	6	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 8.4\text{ A},$ $V_{GS} = 5\text{ V}$		5.4	7.6	nC
$Q_{gs}$	Gate-Source Charge			1.7		nC
$Q_{gd}$	Gate-Drain Charge			1.9		nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current				2.1	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.77	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 8.4\text{ A}, d_I/d_t = 100\text{ A}/\mu\text{s}$		19		ns
$Q_{rr}$	Diode Reverse Recovery Charge			9		nC

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- a)  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



- b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2 Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

3 Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 7\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$

### Typical Characteristics

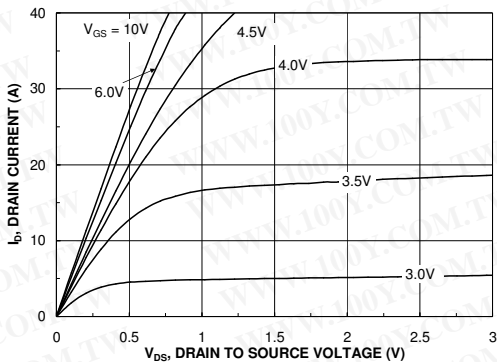


Figure 1. On-Region Characteristics.

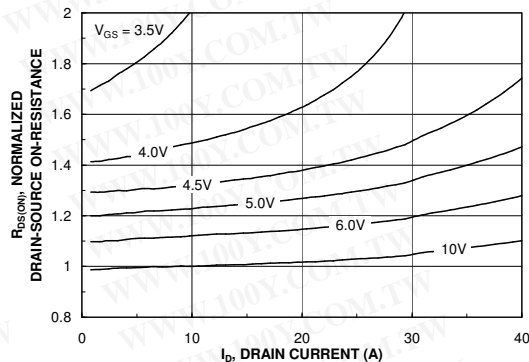


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

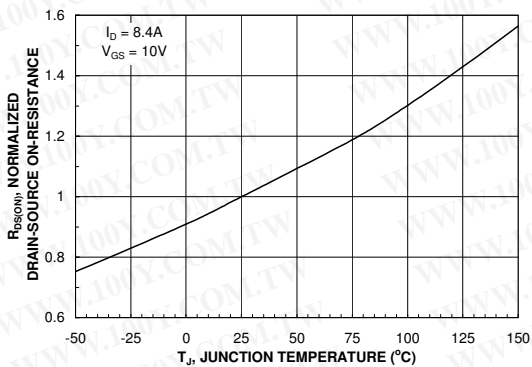


Figure 3. On-Resistance Variation with Temperature.

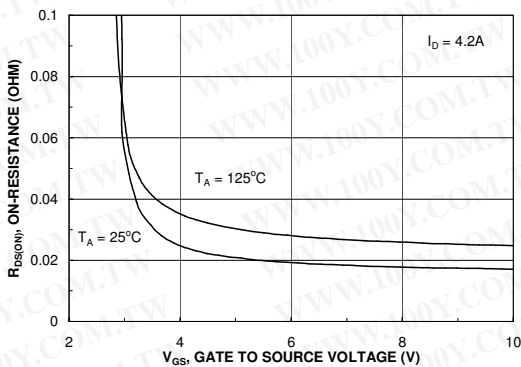


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

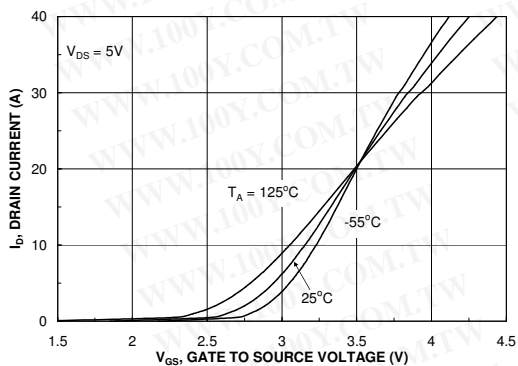


Figure 5. Transfer Characteristics.

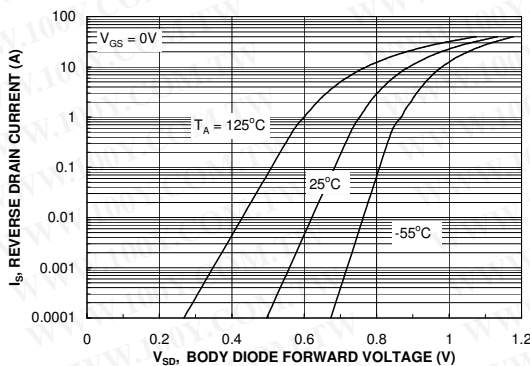


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics

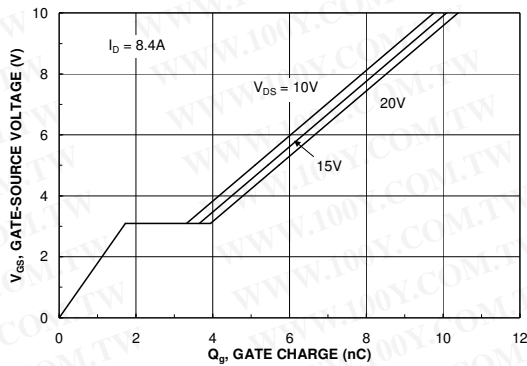


Figure 7. Gate Charge Characteristics.

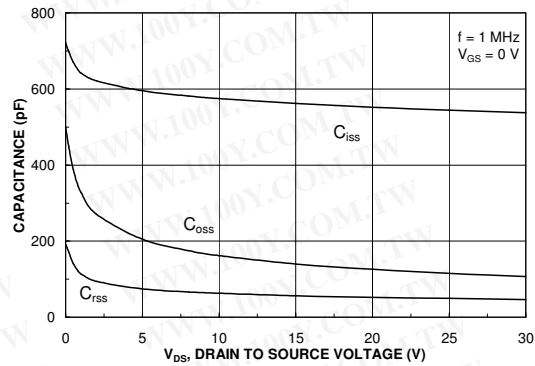


Figure 8. Capacitance Characteristics.

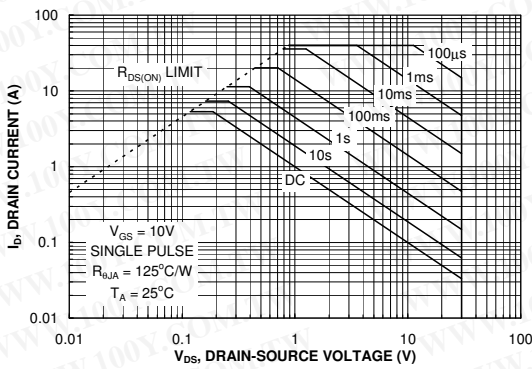


Figure 9. Maximum Safe Operating Area.

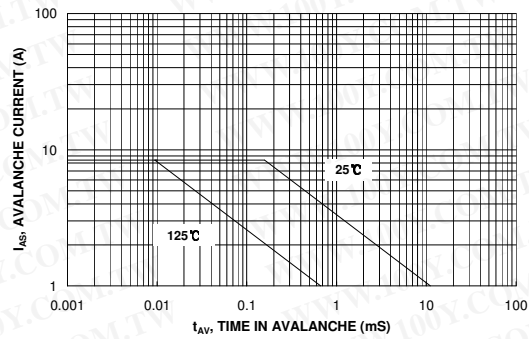


Figure 10. Unclamped Inductive Switching Capability

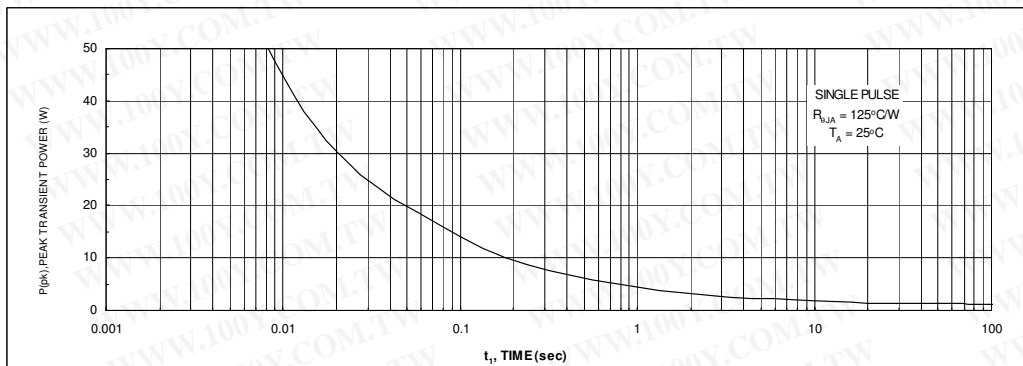
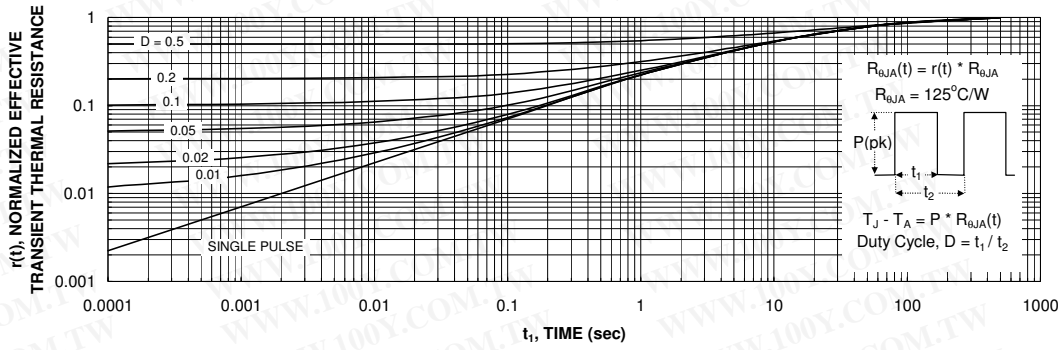


Figure 11. Single Pulse Maximum Power Dissipation.

### Typical Characteristics



**Figure 12. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.  
 Transient thermal response will change depending on the circuit board design.



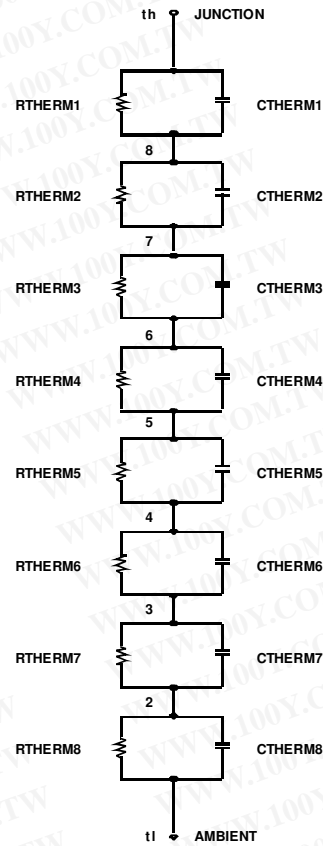
### SPICE Thermal Model

.SUBCKT FDS6612A\_THERM TH TL  
 \*THERMAL MODEL SUBCIRCUIT  
 \*REV A - JULY 2003  
 \*MIN PAD RJA

CTHERM1	TH	8	0.005
CTHERM2	8	7	0.05
CTHERM3	7	6	0.10
CTHERM4	6	5	0.35
CTHERM5	5	4	0.45
CTHERM6	4	3	0.50
CTHERM7	3	2	0.55
CTHERM8	2	TL	3.00

RTHERM1	TH	8	5.000
RTHERM2	8	7	6.250
RTHERM3	7	6	7.500
RTHERM4	6	5	8.750
RTHERM5	5	4	10.625
RTHERM6	4	3	11.875
RTHERM7	3	2	31.250
RTHERM8	2	TL	43.750

.ENDS



FDS6612A Single N-Channel, Logic-Level, PowerTrench<sup>®</sup> MOSFET

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