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FDMA1029PZ

Dual P-Channel PowerTrench[®] MOSFET

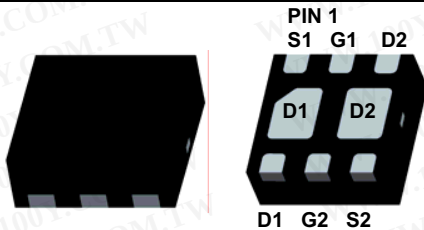
General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable applications. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. When connected in the typical common source configuration, bi-directional current flow is possible.

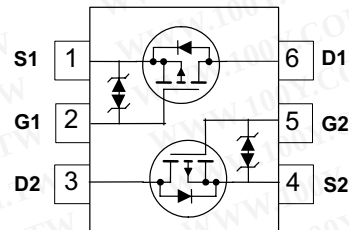
The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- -3.1 A, -20V. $R_{DS(ON)} = 95 \text{ m}\Omega @ V_{GS} = -4.5\text{V}$
 $R_{DS(ON)} = 141 \text{ m}\Omega @ V_{GS} = -2.5\text{V}$
- Low profile – 0.8 mm maximum – in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2.5kV (Note 3)
- RoHS Compliant
- Free from halogenated compounds and antimony oxides



MicroFET 2x2



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous (Note 1a)	-3.1	A
	– Pulsed	-6	
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.4	W
		0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	86 (Single Operation)	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	173 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	69 (Dual Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1d)	151 (Dual Operation)	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
029	FDMA1029PZ	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = −250 μA	−20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = −250 μA, Referenced to 25°C		−12		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = −16 V, V _{GS} = 0 V			−1	μA
I _{GSS}	Gate–Body Leakage	V _{GS} = ± 12 V, V _{DS} = 0 V			±10	μA
On Characteristics (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = −250 μA	−0.6	−1.0	−1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = −250 μA, Referenced to 25°C		4		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = −4.5 V, I _D = −3.1 A V _{GS} = −2.5 V, I _D = −2.5 A V _{GS} = −4.5 V, I _D = −3.1 A, T _J =125°C		60 88 87	95 141 140	mΩ
g _{FS}	Forward Transconductance	V _{DS} = −10 V, I _D = −3.1 A		−11		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = −10 V, V _{GS} = 0 V, f = 1.0 MHz		540		pF
C _{oss}	Output Capacitance			120		pF
C _{rss}	Reverse Transfer Capacitance			100		pF
Switching Characteristics (Note 2)						
t _{d(on)}	Turn–On Delay Time	V _{DD} = −10 V, I _D = −1 A, V _{GS} = −4.5 V, R _{GEN} = 6 Ω		13	24	ns
t _r	Turn–On Rise Time			11	20	ns
t _{d(off)}	Turn–Off Delay Time			37	59	ns
t _f	Turn–Off Fall Time			36	58	ns
Q _g	Total Gate Charge	V _{DS} = −10 V, I _D = −3.1 A, V _{GS} = −4.5 V		7.0	10	nC
Q _{gs}	Gate–Source Charge			1.1		nC
Q _{gd}	Gate–Drain Charge			2.4		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Source–Drain Diode Forward Current				−1.1	A
V _{SD}	Source–Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = −1.1 A (Note 2)		−0.8	−1.2	V
t _{rr}	Diode Reverse Recovery Time	I _F = −3.1 A, dI _F /dt = 100 A/μs		25		ns
Q _{rr}	Diode Reverse Recovery Charge			9		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

(a) $R_{\theta JA} = 86\text{ }^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.

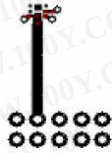
(b) $R_{\theta JA} = 173\text{ }^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper. For single operation.

(c) $R_{\theta JA} = 69\text{ }^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.

(d) $R_{\theta JA} = 151\text{ }^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper. For dual operation.



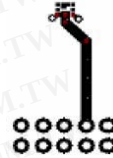
a) 86 $^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper.



b) 173 $^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper.



c) 69 $^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper.



d) 151 $^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

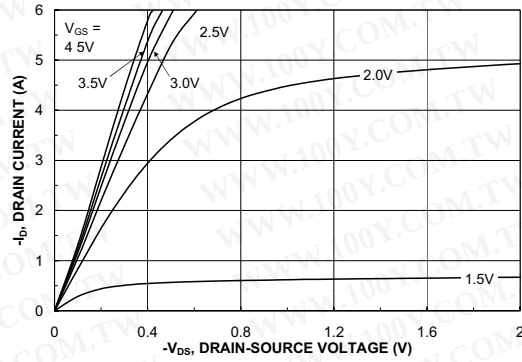


Figure 1. On-Region Characteristics.

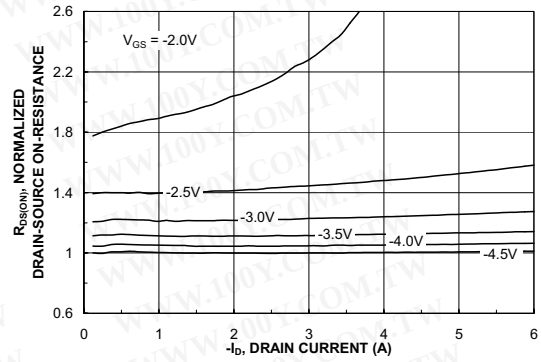


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

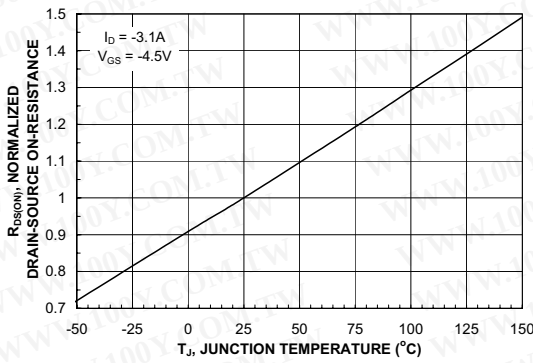


Figure 3. On-Resistance Variation with Temperature.

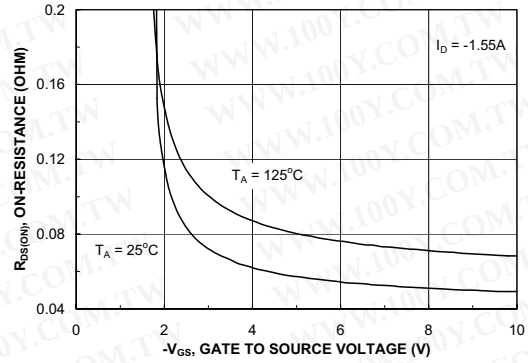


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

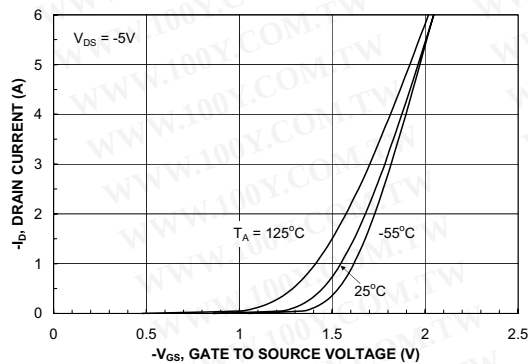


Figure 5. Transfer Characteristics.

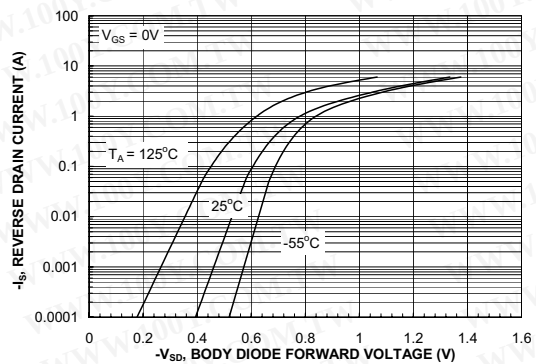


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

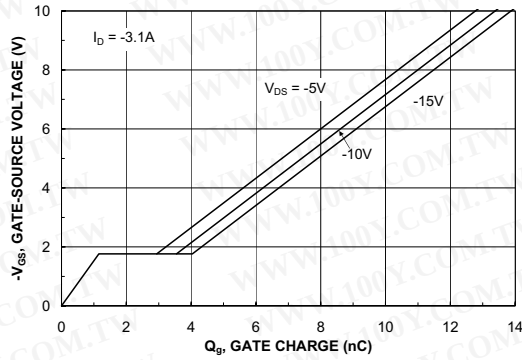


Figure 7. Gate Charge Characteristics.

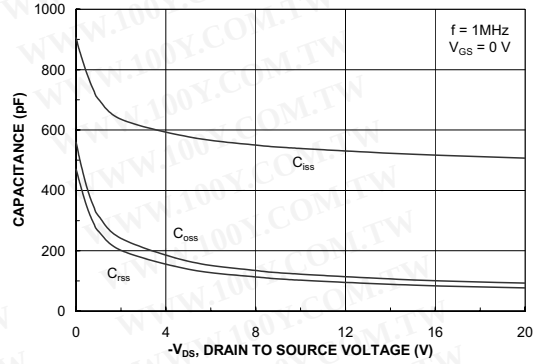


Figure 8. Capacitance Characteristics.

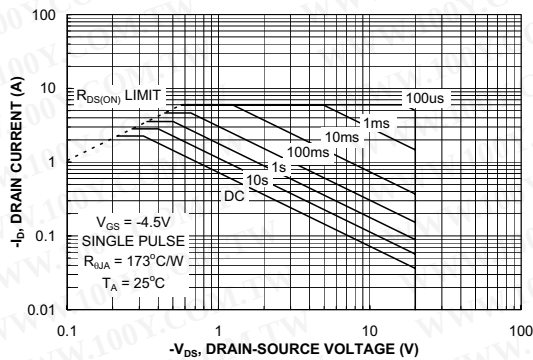


Figure 9. Maximum Safe Operating Area.

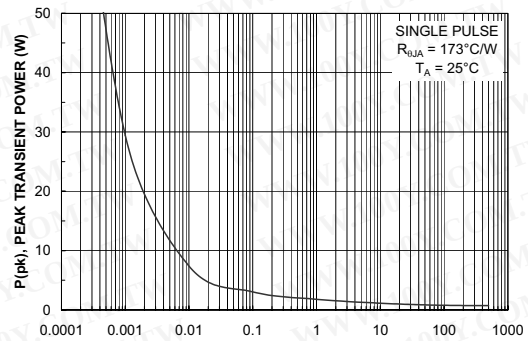


Figure 10. Single Pulse Maximum Power Dissipation.

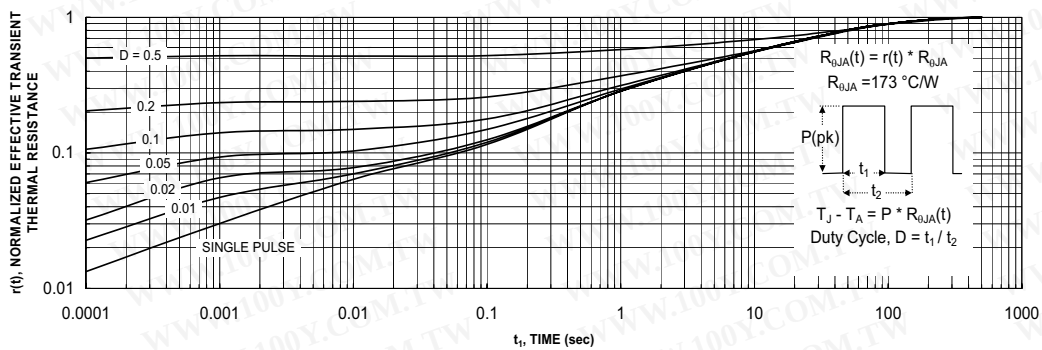
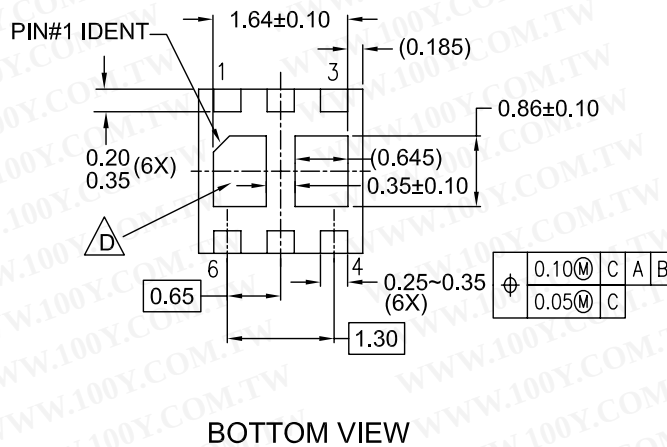
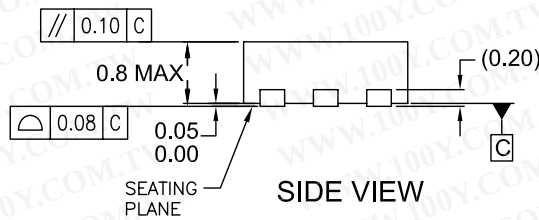
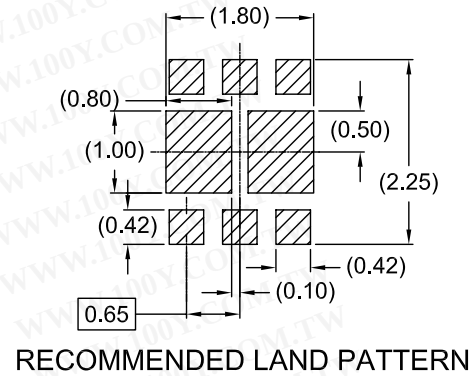
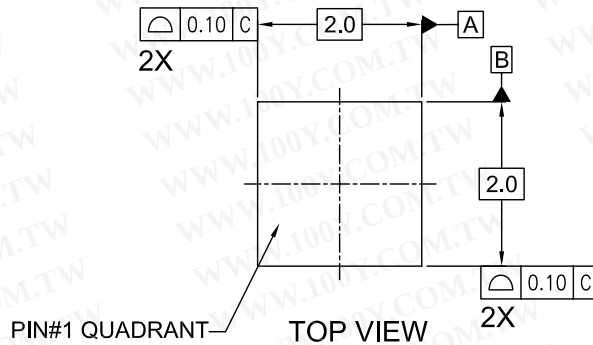


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC EXCEPT AS NOTED.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. NON-JEDEC DUAL DAP
- E. DRAWING FILE NAME : MLP06J rev3

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I40

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