

# FDD8424H

## Dual N & P-Channel PowerTrench® MOSFET N-Channel: 40V, 20A, 24mΩ P-Channel: -40V, -20A, 54mΩ

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 24mΩ at  $V_{GS} = 10V$ ,  $I_D = 9.0A$
- Max  $r_{DS(on)}$  = 30mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 7.0A$

Q2: P-Channel

- Max  $r_{DS(on)}$  = 54mΩ at  $V_{GS} = -10V$ ,  $I_D = -6.5A$
- Max  $r_{DS(on)}$  = 70mΩ at  $V_{GS} = -4.5V$ ,  $I_D = -5.6A$
- Fast switching speed
- RoHS Compliant

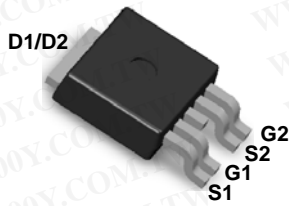


### General Description

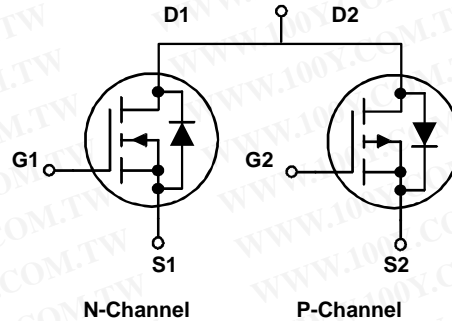
These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench- process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

### Application

- Inverter
- H-Bridge



Dual DPAK 4L



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	40	-40	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current - Continuous (Package Limited)	20	-20	A
	- Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$	26	-20	
	- Continuous $T_A = 25^\circ\text{C}$	9.0	-6.5	
	- Pulsed	55	-40	
$P_D$	Power Dissipation for Single Operation $T_C = 25^\circ\text{C}$ (Note 1)	30	35	W
	$T_A = 25^\circ\text{C}$ (Note 1a)	3.1		
	$T_A = 25^\circ\text{C}$ (Note 1b)	1.3		
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	29	33	mJ
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q1 (Note 1)	4.1	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q2 (Note 1)	3.5	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8424H	FDD8424H	TO-252-4L	13"	12mm	2500 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ $I_D = -250\mu\text{A}$ , $V_{GS} = 0\text{V}$	Q1 Q2	40 -40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1 Q2		34 -32		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}$ , $V_{GS} = 0\text{V}$ $V_{DS} = -32\text{V}$ , $V_{GS} = 0\text{V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$ $V_{GS} = V_{DS}$ , $I_D = -250\mu\text{A}$	Q1 Q2	1 -1	1.7 -1.6	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1 Q2		-5.3 4.8		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 9.0\text{A}$ $V_{GS} = 4.5\text{V}$ , $I_D = 7.0\text{A}$ $V_{GS} = 10\text{V}$ , $I_D = 9.0\text{A}$ , $T_J = 125^\circ\text{C}$	Q1		19 23 29	24 30 37	m $\Omega$
		$V_{GS} = -10\text{V}$ , $I_D = -6.5\text{A}$ $V_{GS} = -4.5\text{V}$ , $I_D = -5.6\text{A}$ $V_{GS} = -10\text{V}$ , $I_D = -6.5\text{A}$ , $T_J = 125^\circ\text{C}$	Q2		42 58 62	54 70 80	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{V}$ , $I_D = 9.0\text{A}$ $V_{DS} = -5\text{V}$ , $I_D = -6.5\text{A}$	Q1 Q2		29 13		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 20\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	Q1 Q2		750 1000	1000 1330	pF
$C_{oss}$	Output Capacitance	Q2	Q1 Q2		115 140	155 185	pF
$C_{riss}$	Reverse Transfer Capacitance	$V_{DS} = -20\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	Q1 Q2		75 75	115 115	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$	Q1		1.1		$\Omega$
			Q2		3.3		

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1	Q1 Q2		7 7	14 14	ns
$t_r$	Rise Time	$V_{DD} = 20\text{V}$ , $I_D = 9.0\text{A}$ , $V_{GS} = 10\text{V}$ , $R_{GEN} = 6\Omega$	Q1		13	24	ns
			Q2		3	10	
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -20\text{V}$ , $I_D = -6.5\text{A}$ , $V_{GS} = -10\text{V}$ , $R_{GEN} = 6\Omega$	Q1		17	31	ns
			Q2		20	36	
$t_f$	Fall Time	$V_{GS} = -10\text{V}$ , $R_{GEN} = 6\Omega$	Q1		6	12	ns
			Q2		3	10	
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{V}$ , $V_{DD} = 20\text{V}$ , $I_D = 9.0\text{A}$	Q1		14	20	nC
			Q2		17	24	
$Q_{gs}$	Gate to Source Charge	Q2	Q1		2.3		nC
			Q2		3.0		
$Q_{gd}$	Gate to Drain "Miller" Charge	$V_{GS} = -10\text{V}$ , $V_{DD} = -20\text{V}$ , $I_D = -6.5\text{A}$	Q1		3.2		nC
			Q2		3.6		

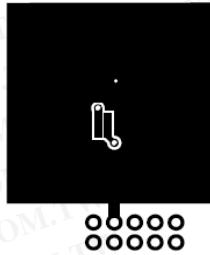
## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics</b>							
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 9.0A$ (Note 2)	Q1	0.87	1.2		V
		$V_{GS} = 0V, I_S = -6.5A$ (Note 2)	Q2	0.88	-1.2		
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 9.0A, di/dt = 100A/s$	Q1	25	38		ns
			Q2	29	44		
$Q_{rr}$	Reverse Recovery Charge	Q2 $I_F = -6.5A, di/dt = 100A/s$	Q1	19	29		nC
			Q2	29	44		

**Notes:**

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

**Q1**



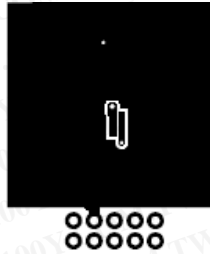
a.  $40^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper

Scale 1 : 1 on letter size paper



b.  $96^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

**Q2**



a.  $40^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper

Scale 1 : 1 on letter size paper



b.  $96^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty cycle < 2.0%.

- Starting  $T_J = 25^\circ\text{C}$ , N-ch:  $L = 0.3\text{mH}$ ,  $I_{AS} = 14A$ ,  $V_{DD} = 40V$ ,  $V_{GS} = 10V$ ; P-ch:  $L = 0.3\text{mH}$ ,  $I_{AS} = -15A$ ,  $V_{DD} = -40V$ ,  $V_{GS} = -10V$ .

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

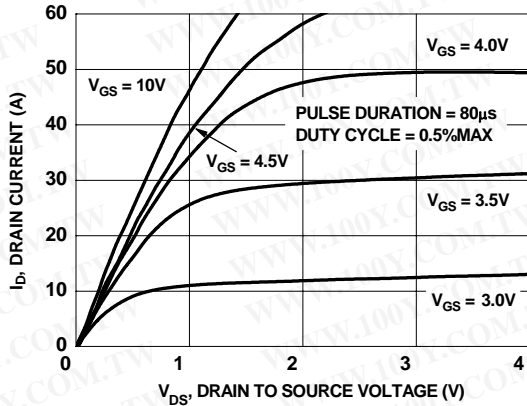


Figure 1. On-Region Characteristics

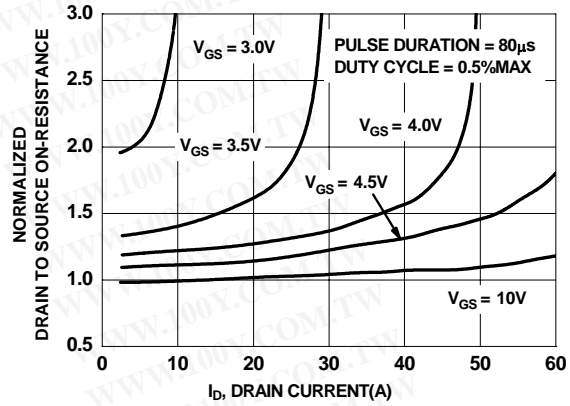


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

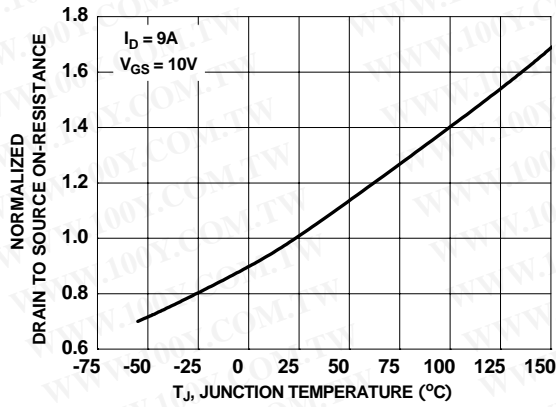


Figure 3. Normalized On-Resistance vs Junction Temperature

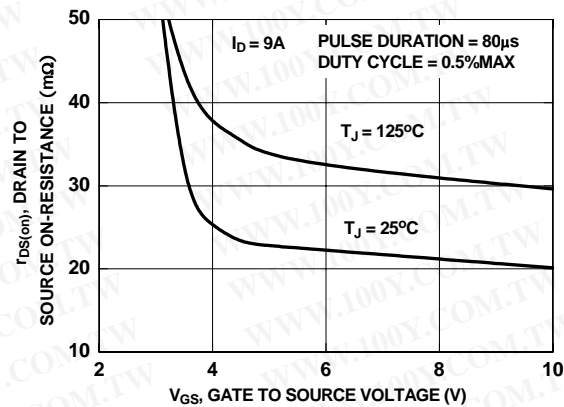


Figure 4. On-Resistance vs Gate to Source Voltage

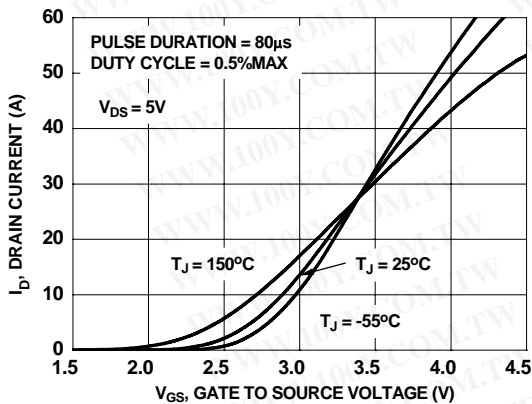


Figure 5. Transfer Characteristics

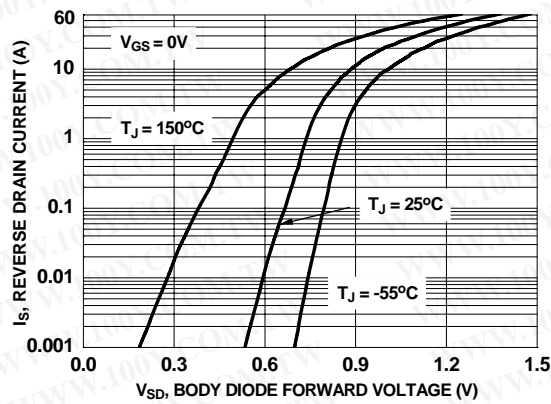
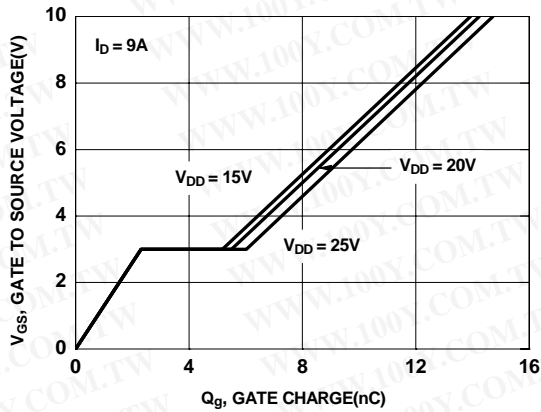
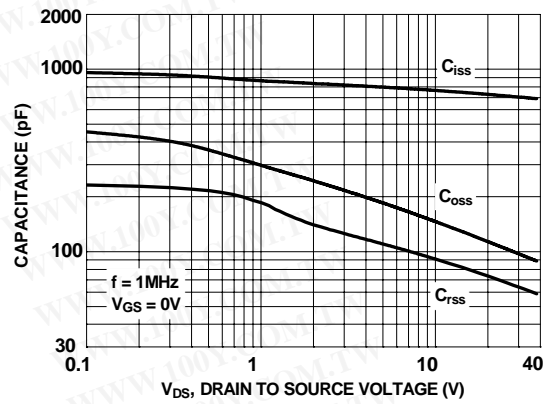


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

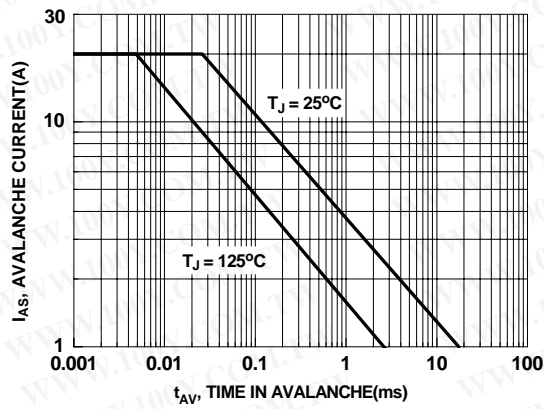
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



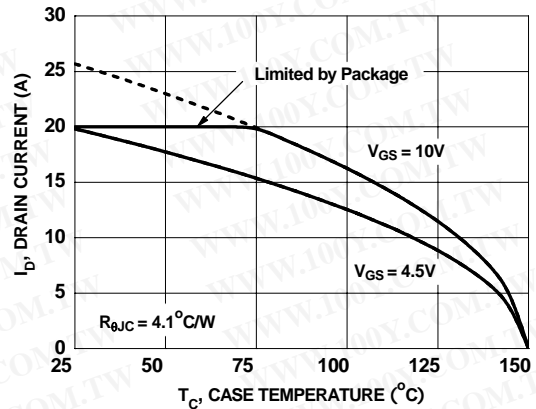
**Figure 7. Gate Charge Characteristics**



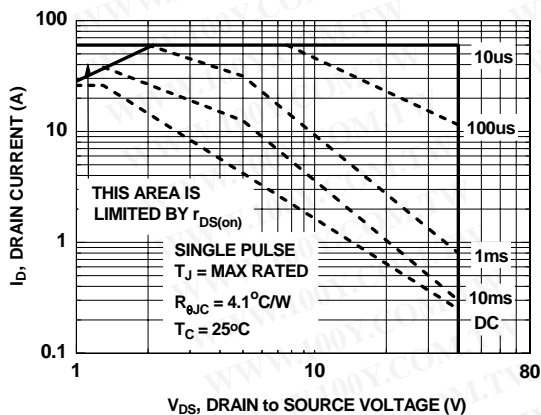
**Figure 8. Capacitance vs Drain to Source Voltage**



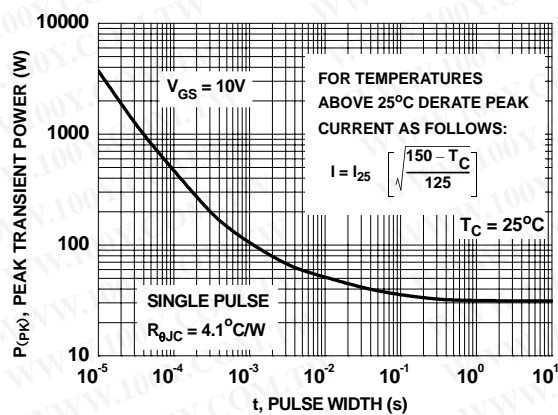
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

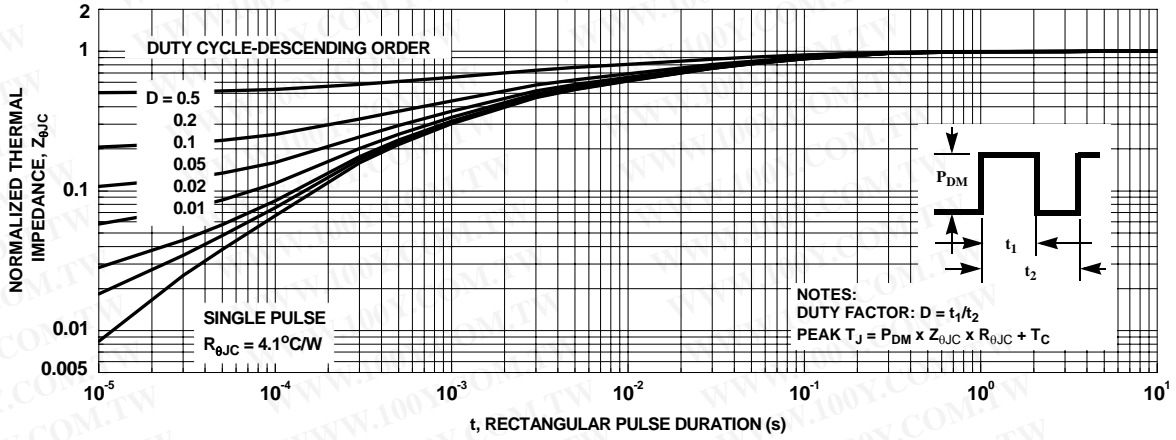


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**



**Typical Characteristics (Q2 P-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

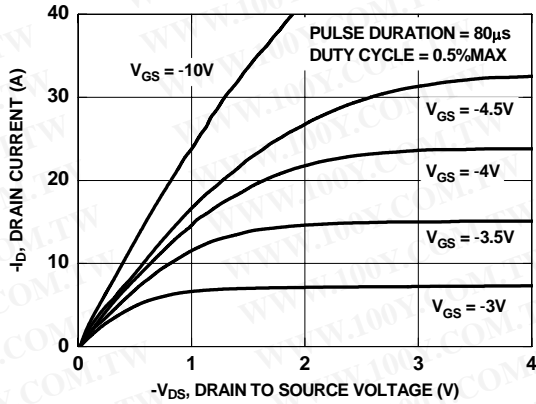


Figure 14. On-Region Characteristics

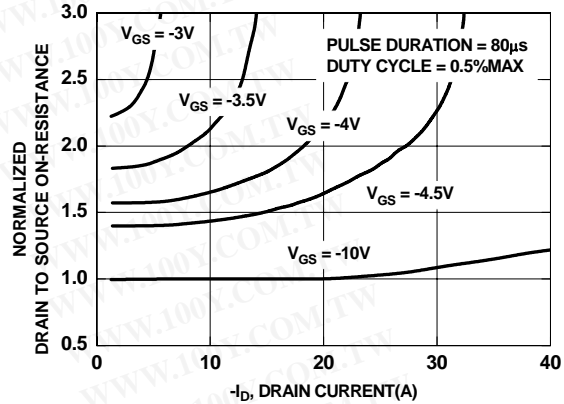


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

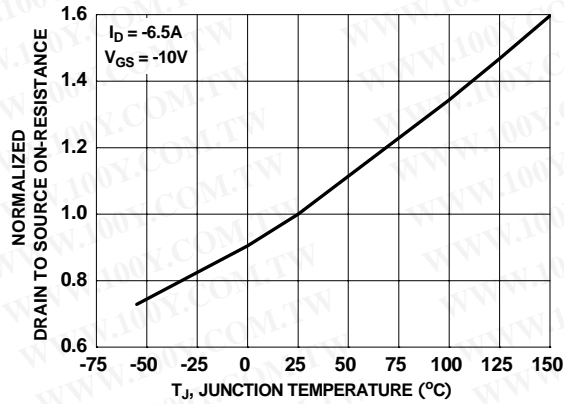


Figure 16. Normalized On-Resistance vs Junction Temperature

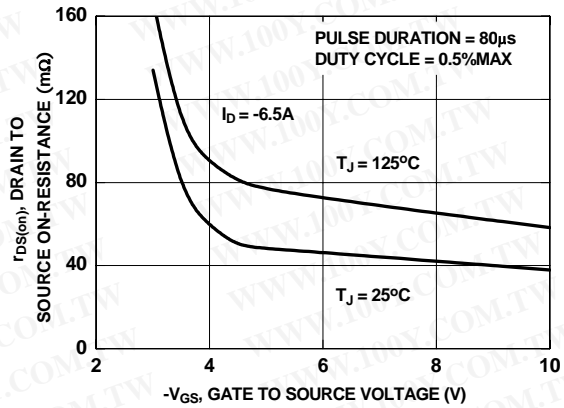


Figure 17. On-Resistance vs Gate to Source Voltage

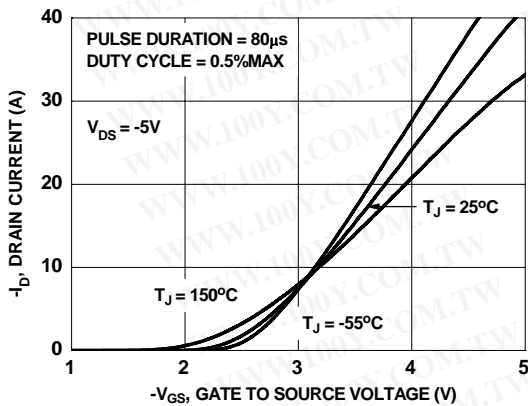


Figure 18. Transfer Characteristics

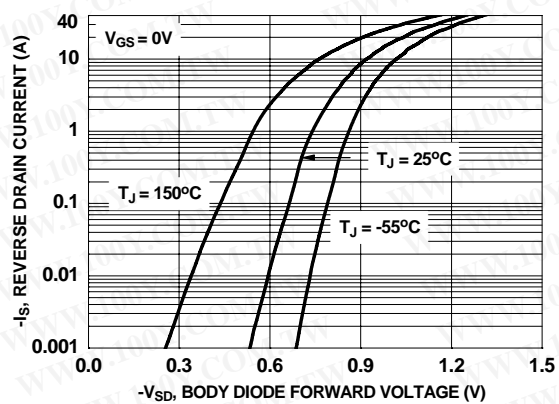
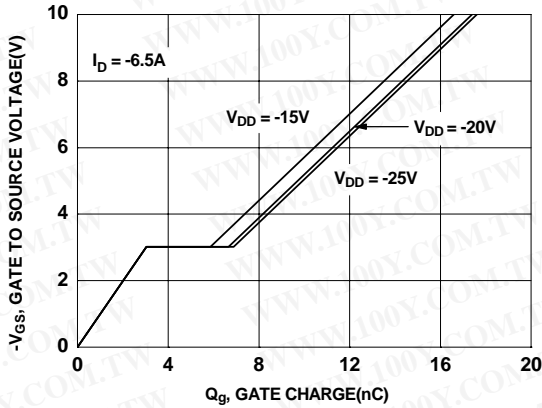
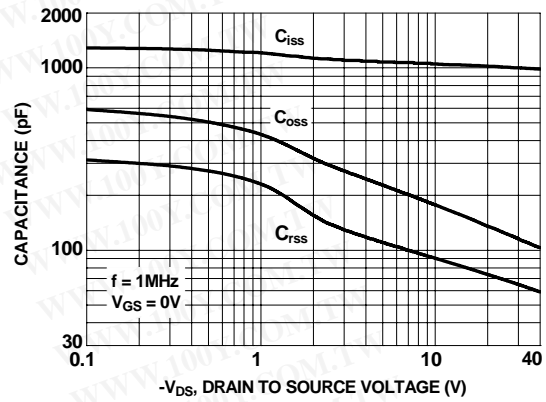


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

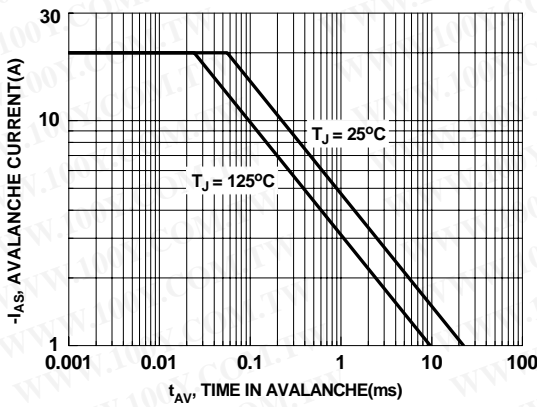
**Typical Characteristics (Q2 P-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



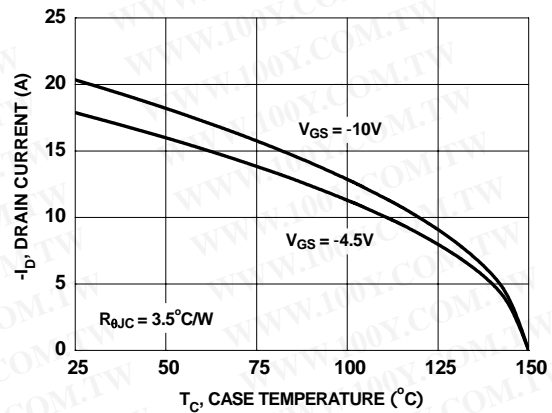
**Figure 20. Gate Charge Characteristics**



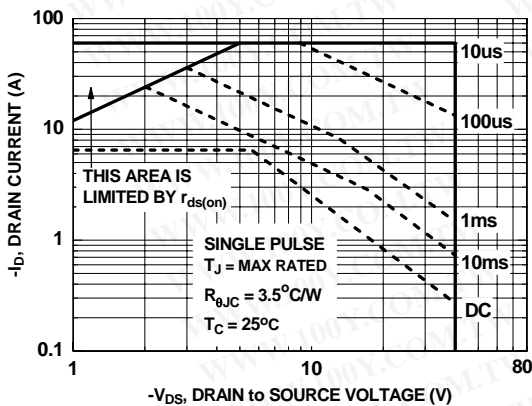
**Figure 21. Capacitance vs Drain to Source Voltage**



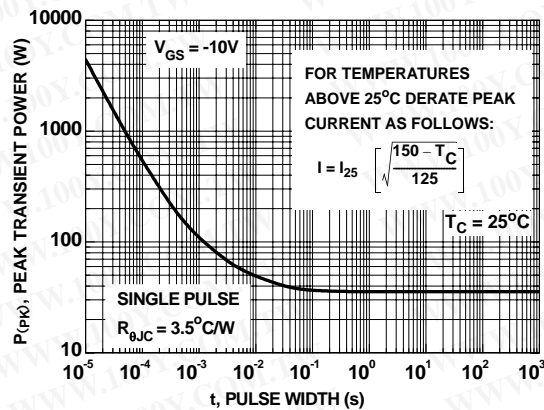
**Figure 22. Unclamped Inductive Switching Capability**



**Figure 23. Maximum Continuous Drain Current vs Case Temperature**

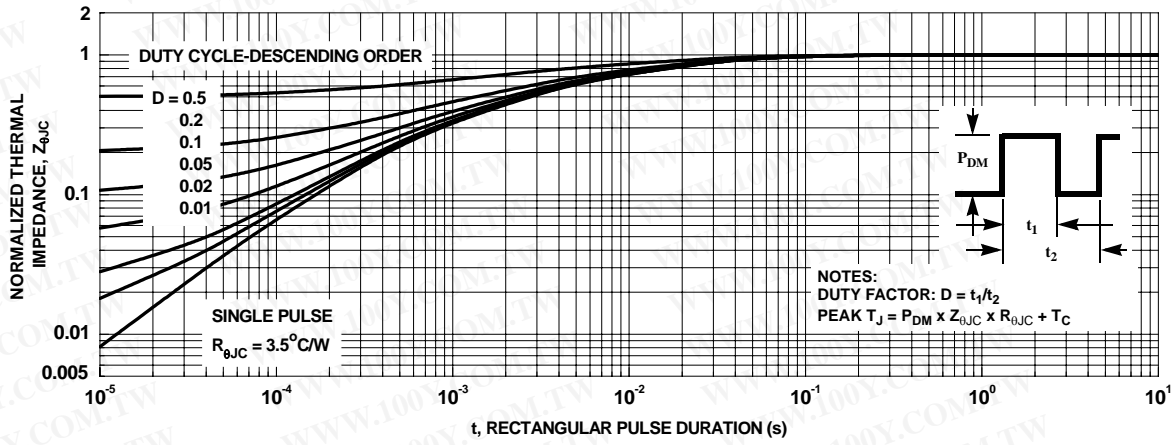


**Figure 24. Forward Bias Safe Operating Area**

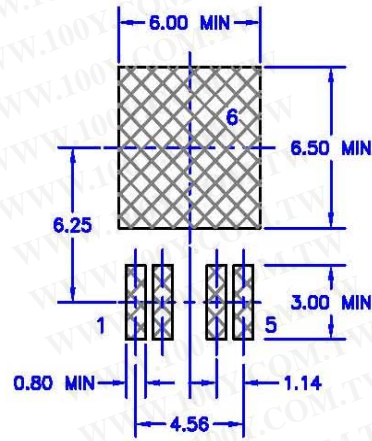
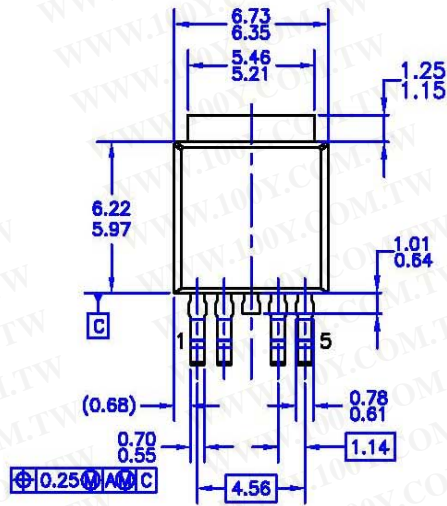


**Figure 25. Single Pulse Maximum Power Dissipation**

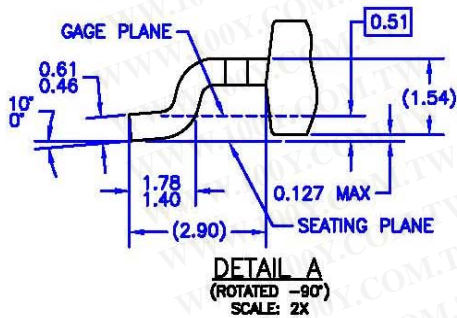
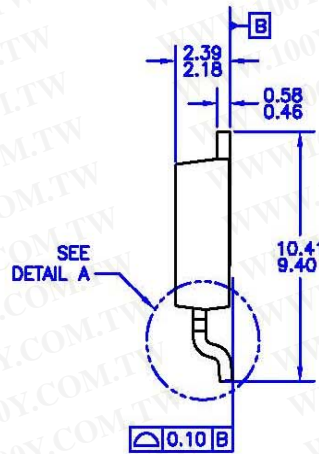
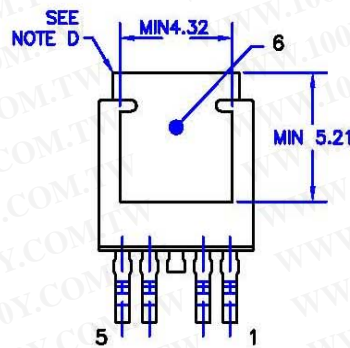
**Typical Characteristics (Q2 P-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 26. Transient Thermal Response Curve**



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252 ISSUE E, VARIATION AD, DATED JUNE, 2004.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERD CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

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Bottomless™	IntelliMAX™	QT Optoelectronics™	TinyWire™
Build it Now™	ISOPLANAR™	Quiet Series™	TruTranslation™
CoolFET™	MICROCOUPLER™	RapidConfigure™	µSerDes™
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CTL™	MICROWIRE™	ScalarPump™	UniFET™
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EnSigna™	OPTOLOGIC®	SuperSOT™-3	
FACT Quiet Series™	OPTOPLANAR®	SuperSOT™-6	
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2. A critical component in any component of a life support device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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