FAIRCHILD SEMICONDUCTOR®

July 2008

UniFET™

# FDB52N20
# 200V N-Channel MOSFET



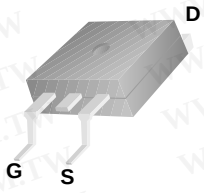
## Features

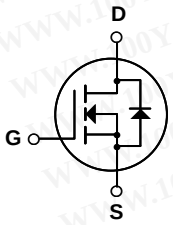
- 52A, 200V, $R_{DS(on)}$ = 0.049Ω @$V_{GS}$ = 10 V
- Low gate charge ( typical 49 nC)
- Low $C_{rss}$ ( typical 66 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

## Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.




## Absolute Maximum Ratings

| Symbol | Parameter | | FDB52N20 | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 200 | V |
| $I_D$ | Drain Current | - Continuous ($T_C$ = 25°C)<br>- Continuous ($T_C$ = 100°C) | 52<br>33 | A<br>A |
| $I_{DM}$ | Drain Current | - Pulsed (Note 1) | 208 | A |
| $V_{GSS}$ | Gate-Source voltage | | ±30 | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 2520 | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | 52 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 35.7 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 4.5 | V/ns |
| $P_D$ | Power Dissipation | ($T_C$ = 25°C)<br>- Derate above 25°C | 357<br>2.86 | W<br>W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | °C |
| $T_L$ | Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds | | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | -- | 0.35 | °C/W |
| $R_{\theta JA}$* | Thermal Resistance, Junction-to-Ambient* | -- | 40 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | -- | 62.5 | °C/W |

* When mounted on the minimum pad size recommended (PCB Mount)

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDB52N20 | FDB52N20TM | $D^2$-PAK | 330mm | 24mm | 800 |

## Electrical Characteristics $T_C$ = 25°C unless otherwise noted

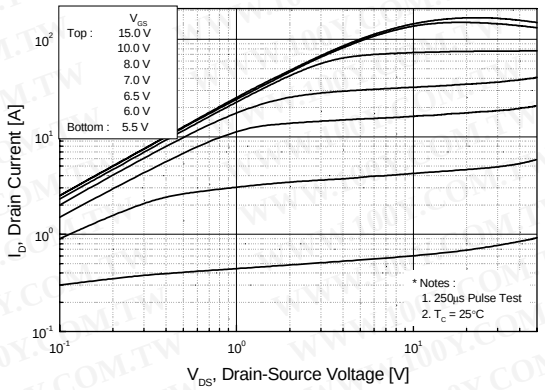
| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = 250µA | 200 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250µA, Referenced to 25°C | -- | 0.2 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 200V, $V_{GS}$ = 0V<br>$V_{DS}$ = 160V, $T_C$ = 125°C | --<br>-- | --<br>-- | 1<br>10 | µA<br>µA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 30V, $V_{DS}$ = 0V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -30V, $V_{DS}$ = 0V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA | 3.0 | -- | 5.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10V, $I_D$ = 26A | -- | 0.041 | 0.049 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 40V, $I_D$ = 26A (Note 4) | -- | 35 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1.0MHz | -- | 2230 | 2900 | pF |
| $C_{oss}$ | Output Capacitance | | -- | 540 | 700 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 66 | 100 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 100V, $I_D$ = 52A<br>$R_G$ = 25Ω | -- | 53 | 115 | ns |
| $t_r$ | Turn-On Rise Time | | -- | 175 | 359 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 48 | 107 | ns |
| $t_f$ | Turn-Off Fall Time | (Note 4, 5) | -- | 29 | 68 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 160V, $I_D$ = 52A<br>$V_{GS}$ = 10V | -- | 49 | 63 | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 19 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | (Note 4, 5) | -- | 24 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 52 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 204 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0V, $I_S$ = 52A | -- | -- | 1.4 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0V, $I_S$ = 52A<br>$dI_F/dt$ =100A/µs (Note 4) | -- | 162 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 1.3 | -- | µC |

**NOTES:**

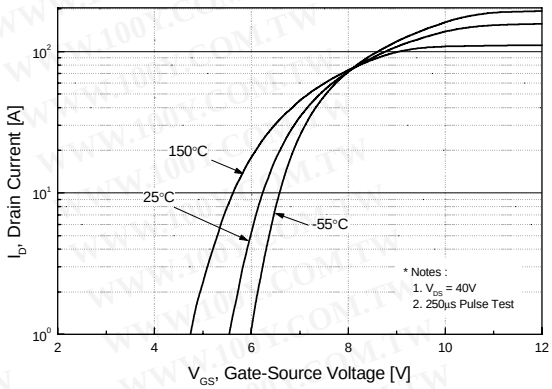
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 1.4mH, $I_{AS}$ = 52A, $V_{DD}$ = 50V, $R_G$ = 25Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 52A, di/dt ≤ 200A/µs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

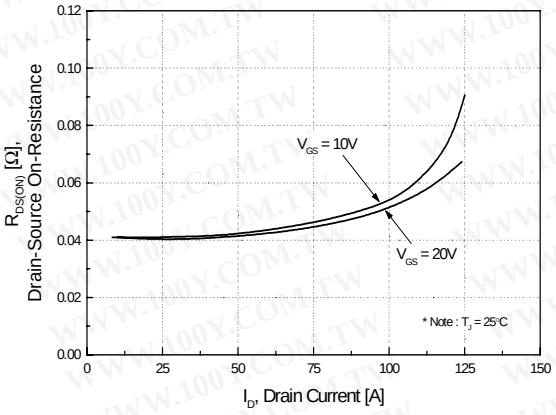
### Figure 1. On-Region Characteristics



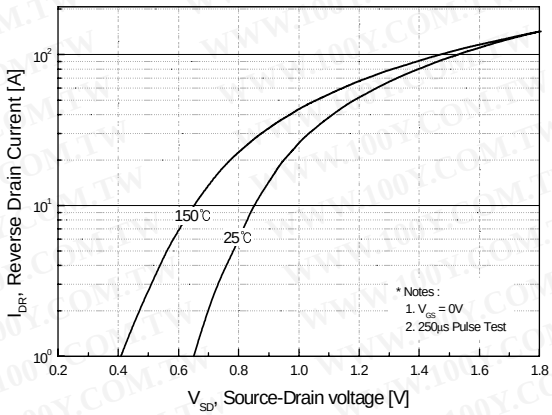

### Figure 2. Transfer Characteristics



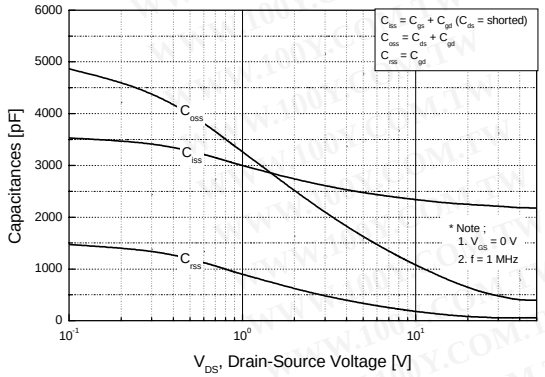

### Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage



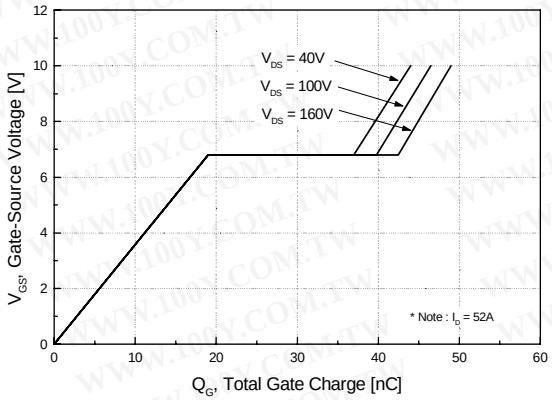

### Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue




### Figure 5. Capacitance Characteristics




### Figure 6. Gate Charge Characteristics



## Typical Performance Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation vs. Temperature**

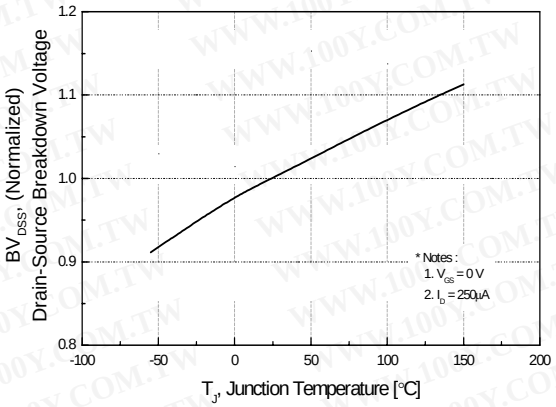



**Figure 8. On-Resistance Variation vs. Temperature**

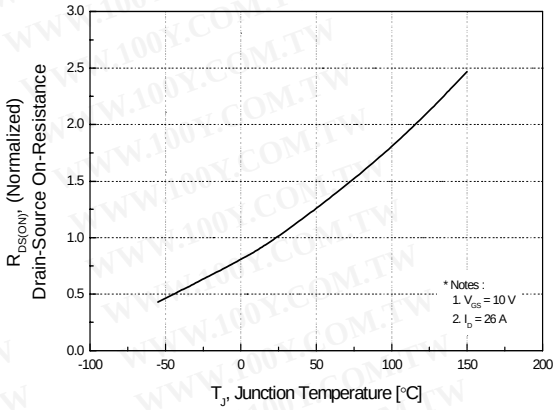



**Figure 9. Maximum Safe Operating Area**

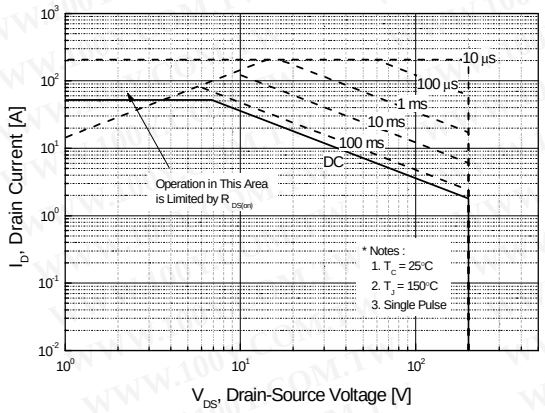



**Figure 10. Maximum Drain Current vs. Case Temperature**

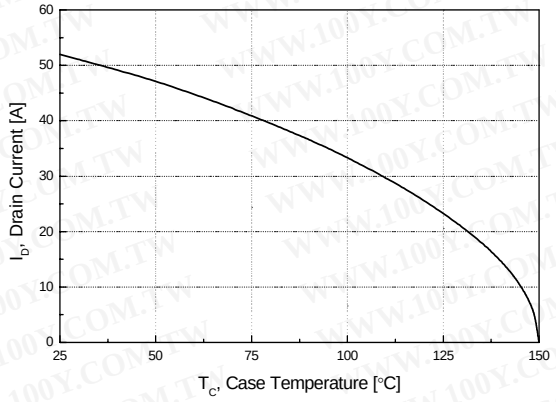
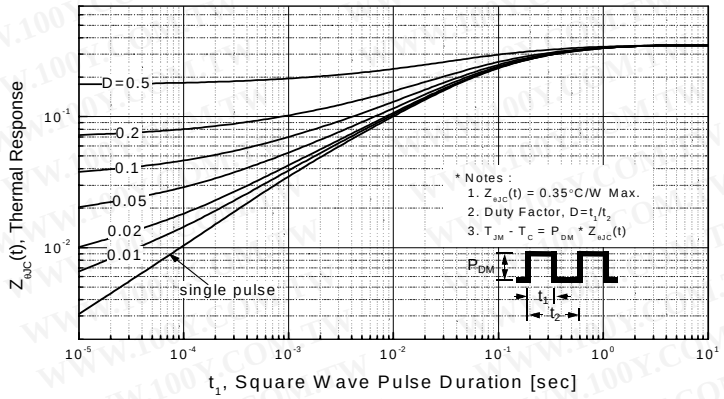
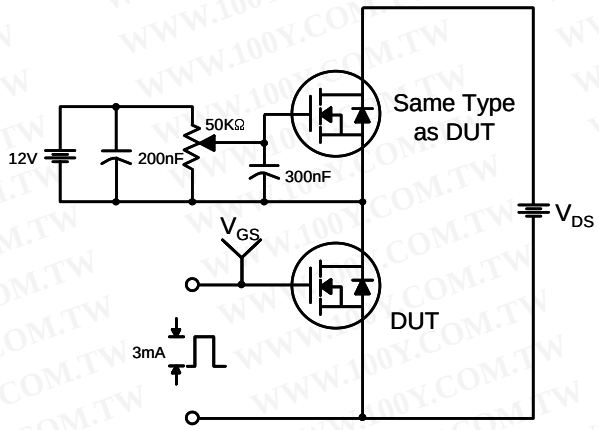
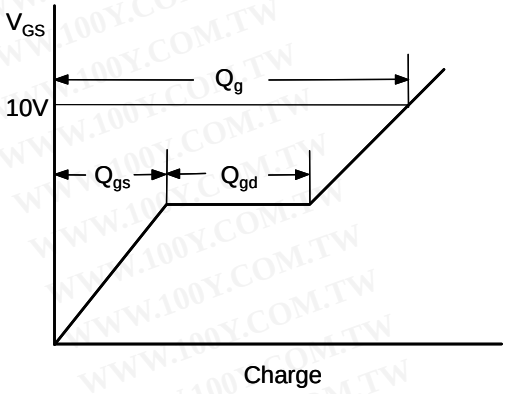



**Figure 11. Transient Thermal Response Curve**

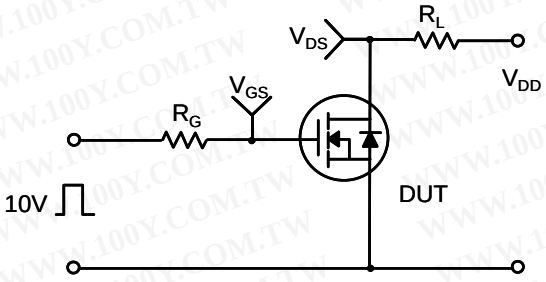


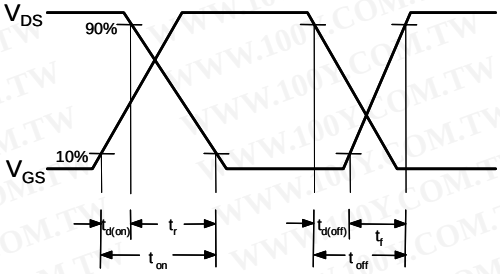
## Gate Charge Test Circuit & Waveform



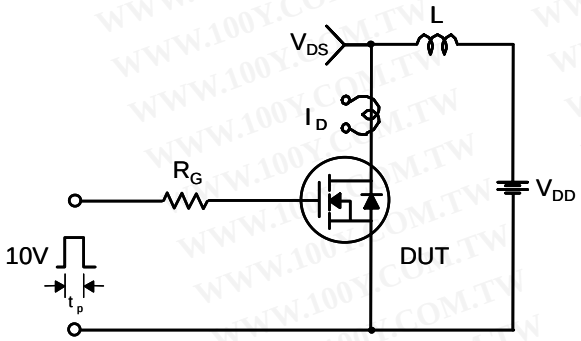




## Resistive Switching Test Circuit & Waveforms

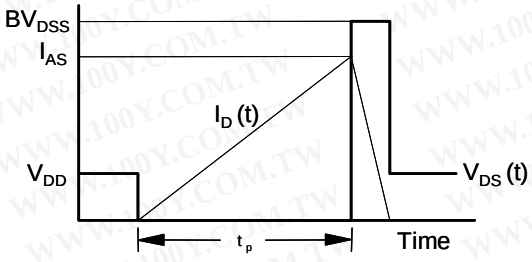


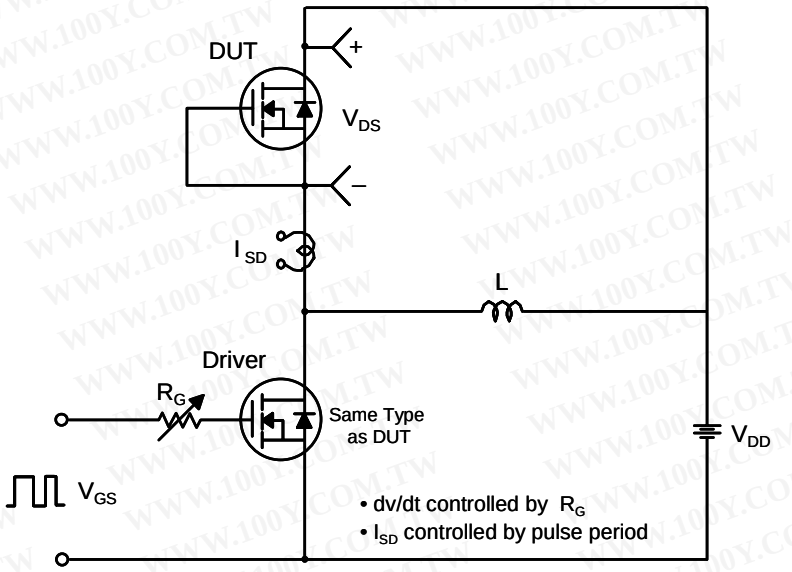

## Unclamped Inductive Switching Test Circuit & Waveforms

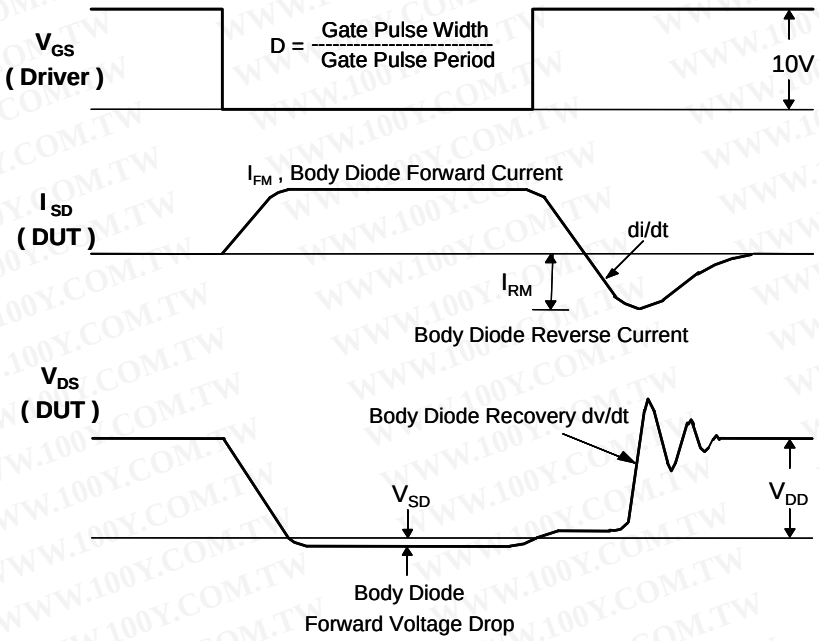



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



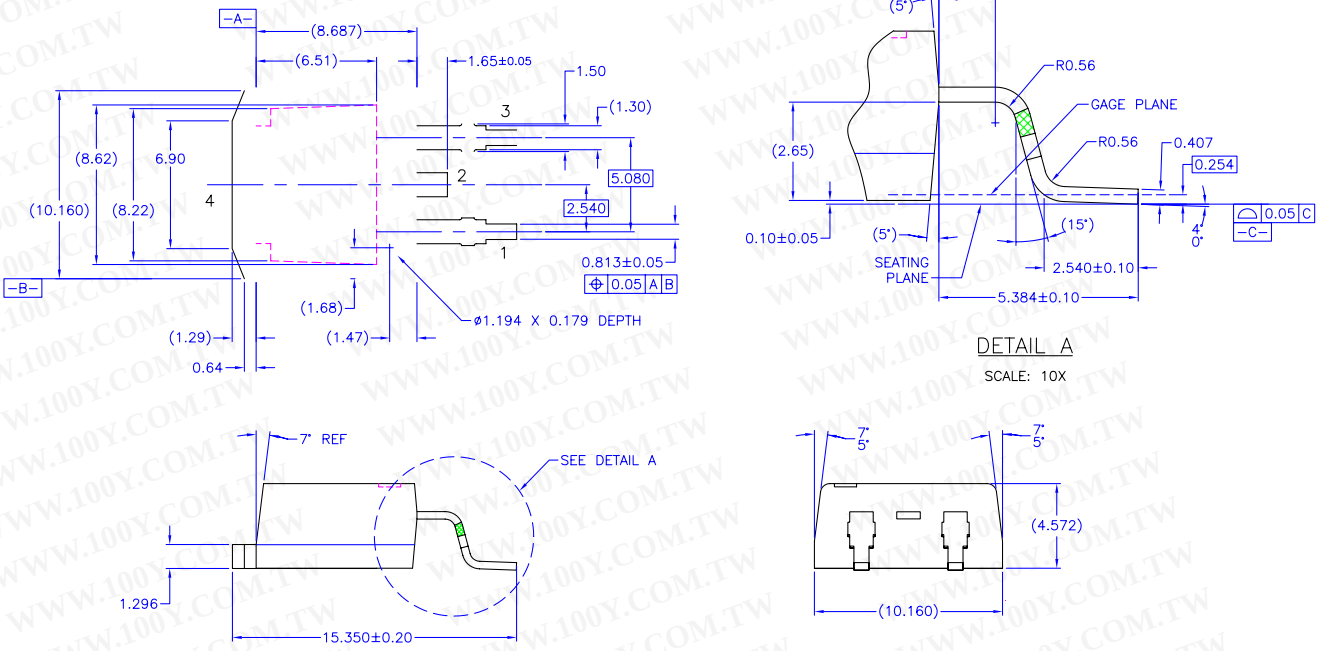
## Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions

# D2-PAK

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A) STANDARD LEAD FINISH: 200 MICROINCHES / 5.08 MICROMETERS MIN. 85Sn15Pb / MATTE Sn (LEAD FREE) ON LEADFRAME MATERIAL.
B) MAXIMUM VERTICAL BURR ON LEAD TIPS NOT TO EXCEED 0.05MM FACING UP. VERTICAL LEAD TIP BURR DOWN SHOULD BE ZERO.
C) NO PACKAGE CHIPS, CRACKS OR SURFACE INDENTION ALLOWED AFTER FORMING.
D) DOCUMENT REFERENCE:
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MOLDED PACKAGE: (CB)41-0100, TO-263, 3 LDS, SUZHOU, IDF

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