

### FEATURES

- Very Low Voltage Noise ..... @ 100Hz,  $1\text{nV}/\sqrt{\text{Hz}}$  MAX
- Excellent Current Gain Match ..... 0.5% TYP
- Tight  $V_{BE}$  Match ( $V_{OS}$ ) ..... 200 $\mu\text{V}$  MAX
- Outstanding Offset Voltage Drift ..... 0.03 $\mu\text{V}/^\circ\text{C}$  TYP
- High Gain-Bandwidth Product ..... 200MHz TYP
- Low Cost
- Direct Replacement For LM394BN/CN

### ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
SSM2210P	-40°C to +85°C	PDIP	P-8
SSM2210S	-40°C to +85°C	SOIC	S-8
SSM2210S-REEL	-40°C to +85°C	SOIC	S-8

### GENERAL DESCRIPTION

The SSM2210 is a dual NPN matched transistor pair specifically designed to meet the requirements of ultra-low noise audio systems.

With its extremely low input base spreading resistance ( $r_{bb'}$  is typically 28 $\Omega$ ), and high current gain ( $h_{FE}$  typically exceeds 600 @  $I_C = 1\text{mA}$ ), systems implementing the SSM2210 can achieve outstanding signal-to-noise ratios. This will result in superior performance compared to systems incorporating commercially available monolithic amplifiers.

The equivalent input voltage noise of the SSM2210 is typically only 0.8nV/ $\sqrt{\text{Hz}}$  over the entire audio bandwidth of 20Hz to 20KHz.

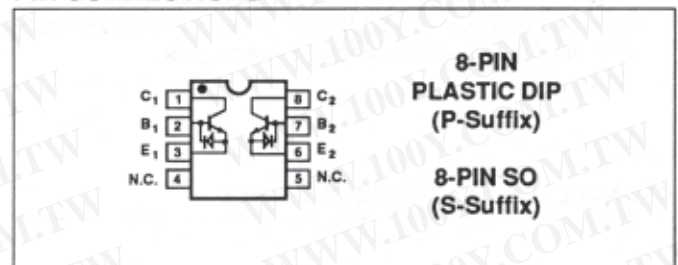
Excellent matching of the current gain ( $\Delta h_{FE}$ ) to about 0.5% and low  $V_{OS}$  of less than 50 $\mu\text{V}$  (typical) make it ideal for symmetrically balanced designs which reduce high order amplifier harmonic distortion.

Stability of the matching parameters is guaranteed by protection diodes across the base-emitter junction. These diodes prevent degradation of Beta and matching characteristics due to reverse biasing of the base-emitter junction.

The SSM2210 is also an ideal choice for accurate and reliable current biasing and mirroring circuits. Furthermore, since a current mirror's accuracy degrades exponentially with mismatches of  $V_{BE}$ 's between transistor pairs, the low  $V_{OS}$  of the SSM2210 will preclude offset trimming in most circuit applications.

The SSM2210 is offered in an 8-pin epoxy DIP and 8-pin SO, its performance and characteristics are guaranteed over the extended industrial temperature range of -40°C to +85°C.

### PIN CONNECTIONS



### ABSOLUTE MAXIMUM RATINGS

Collector Current ( $I_C$ )	20mA
Emitter Current ( $I_E$ )	20mA
Collector-Collector Voltage ( $BV_{CC}$ )	40V
Collector-Base Voltage ( $BV_{CBO}$ )	40V
Collector-Emitter Voltage ( $BV_{CEO}$ )	40V
Emitter-Emitter Voltage ( $BV_{EE}$ )	40V
Operating Temperature Range	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Junction Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

PACKAGE TYPE	$\theta_{JA}$ (NOTE 1)	$\theta_{JC}$	UNITS
8-Pin Plastic DIP (P)	110	50	$^\circ\text{C}/\text{W}$
8-Pin SO (S)	160	44	$^\circ\text{C}/\text{W}$

#### NOTE:

1.  $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for P-DIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO packages.

勝特力材料 886-3-5753170  
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# SSM2210

**ELECTRICAL CHARACTERISTICS** at  $V_{CB} = 15V$ ,  $I_C = 10\mu A$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM2210			UNITS
			MIN	TYP	MAX	
Current Gain	$h_{FE}$	$I_C = 1mA$ (Note 1) $I_C = 10\mu A$	300 200	605 550	– –	
Current Gain Match	$\Delta h_{FE}$	$10\mu A \leq I_C \leq 1mA$ (Note 2)	–	0.5	5	%
Noise Voltage Density	$e_n$	$I_C = 1mA, V_{CB} = 0$ (Note 3) $f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1kHz$ $f_o = 10kHz$	– – – –	1.6 0.9 0.85 0.85	2 1 1 1	nV/ $\sqrt{Hz}$
Offset Voltage	$V_{OS}$	$V_{CB} = 0$ $I_C = 1mA$	–	10	200	$\mu V$
Offset Voltage Change vs $V_{CB}$	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq V_{MAX}$ (Note 4) $1\mu A \leq I_C \leq 1mA$ (Note 5)	–	10	50	$\mu V$
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	$V_{CB} = 0V$ $1\mu A \leq I_C \leq 1mA$ (Note 5)	–	5	70	$\mu V$
Breakdown Voltage	$BV_{CEO}$		40	–	–	V
Gain-Bandwidth Product	$f_T$	$I_C = 10mA, V_{CE} = 10V$	–	200	–	MHz
Collector-Base Leakage Current	$I_{CBO}$	$V_{CB} = V_{MAX}$	–	25	500	$\mu A$
Collector-Collector Leakage Current	$I_{CC}$	$V_{CC} = V_{MAX}$ (Notes 6, 7)	–	35	500	$\mu A$
Collector-Emitter Leakage Current	$I_{CES}$	$V_{CE} = V_{MAX}$ (Notes 6, 7) $V_{BE} = 0$	–	35	500	$\mu A$
Input Bias Current	$I_B$	$I_C = 10\mu A$	–	–	50	nA
Input Offset Current	$I_{OS}$	$I_C = 10\mu A$	–	–	6.2	nA
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1mA$ $I_B = 100\mu A$	–	0.05	0.2	V
Output Capacitance	$C_{OB}$	$V_{CB} = 15V, I_E = 0$	–	23	–	pF
Bulk Resistance	$r_{BE}$	$10\mu A \leq I_C \leq 10mA$ (Note 6)	–	0.3	1.6	$\Omega$
Collector-Collector Capacitance	$C_{CC}$	$V_{CC} = 0$	–	35	–	pF

## NOTES:

- Current gain is guaranteed with Collector-Base Voltage ( $V_{CB}$ ) swept from 0 to  $V_{MAX}$  at the indicated collector currents.
- Current Gain Match ( $\Delta h_{FE}$ ) is defined as:  

$$\Delta h_{FE} = \frac{100(\Delta I_B)(h_{FEmin})}{I_C}$$
- Noise Voltage Density is guaranteed, but not 100% tested.
- This is the maximum change in  $V_{OS}$  as  $V_{CB}$  is swept from 0V to 40V.
- Measured at  $I_C = 10\mu A$  and guaranteed by design over the specified range of  $I_C$ .
- Guaranteed by design.
- $I_{CC}$  and  $I_{CES}$  are verified by measurement of  $I_{CBO}$ .

## ELECTRICAL CHARACTERISTICS at $V_{CB} = 15V, -40^{\circ}C \leq T_A \leq +85^{\circ}C$ , unless otherwise noted.

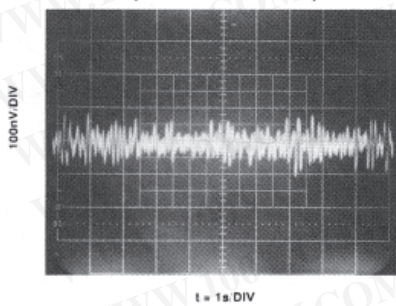
PARAMETER	SYMBOL	CONDITIONS	SSM2210			UNITS
			MIN	TYP	MAX	
Current Gain	$h_{FE}$	$I_C = 1mA$ (Note 1) $I_C = 10\mu A$	300 200	— —	— —	
Offset Voltage	$V_{OS}$	$V_{CB} = 0$ $I_C = 1mA$	—	—	220	$\mu V$
Average Offset Voltage Drift	$TCV_{OS}$	$10\mu A \leq I_C \leq 1mA, 0 \leq V_{CB} \leq V_{MAX}$ (Note 2) $V_{OS}$ Trimmed to Zero (Note 3)	— —	0.08 0.03	1 0.3	$\mu V/^{\circ}C$
Input Bias Current	$I_B$	$I_C = 10\mu A$	—	—	50	nA
Input Offset Current	$I_{OS}$	$I_C = 10\mu A$	—	—	13	nA
Input Offset Current Drift	$TCI_{OS}$	$I_C = 10\mu A$ (Note 4)	—	40	150	$\mu A/^{\circ}C$
Collector-Base Leakage Current	$I_{CBO}$	$V_{CB} = V_{MAX}$	—	3	—	nA
Collector-Emitter Leakage Current	$I_{CES}$	$V_{CE} = V_{MAX}, V_{BE} = 0$	—	4	—	nA
Collector-Collector Leakage Current	$I_{CC}$	$V_{CC} = V_{MAX}$	—	4	—	nA

### NOTES:

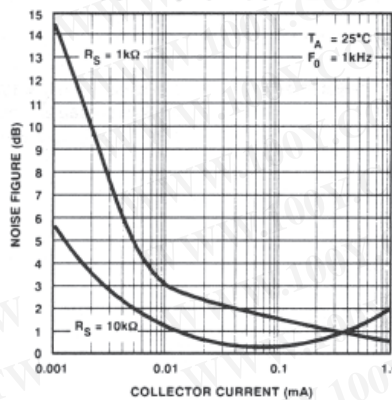
- Current gain is guaranteed with Collector-Base Voltage ( $V_{CB}$ ) swept from 0 to  $V_{MAX}$  at the indicated collector current.
- Guaranteed by  $V_{OS}$  test ( $TCV_{OS} \sim \frac{V_{OS}}{T} \times V_{BE}$ ),  $T = 298K$  for  $T_A = 25^{\circ}C$ .
- The initial zero offset voltage is established by adjusting the ratio of  $I_{C1}$  to  $I_{C2}$  at  $T_A = 25^{\circ}C$ . This ratio must be held to 0.003% over the entire temperature range. Measurements are taken at the temperature extremes and  $25^{\circ}C$ .
- Guaranteed by design.

## TYPICAL PERFORMANCE CHARACTERISTICS

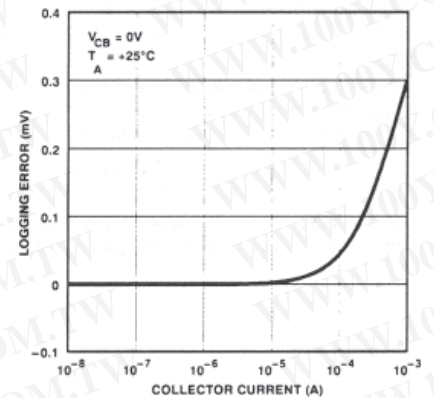
### LOW FREQUENCY NOISE (0.1 Hz TO 10 Hz)



### NOISE FIGURE vs COLLECTOR CURRENT

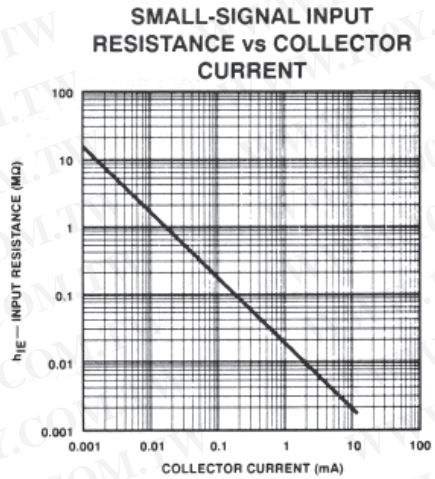
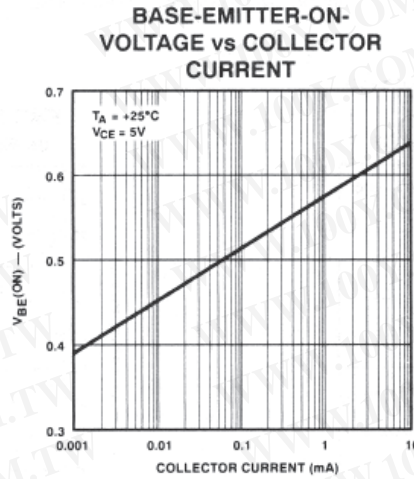
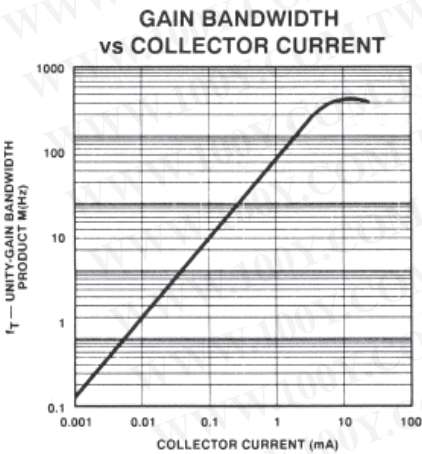
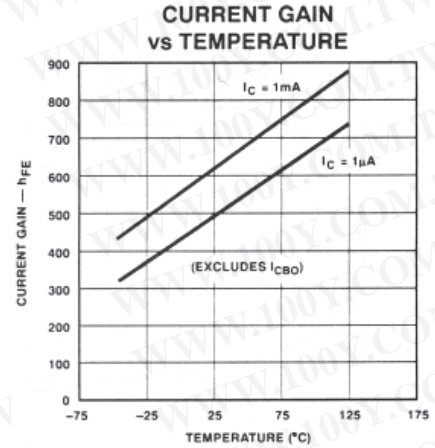
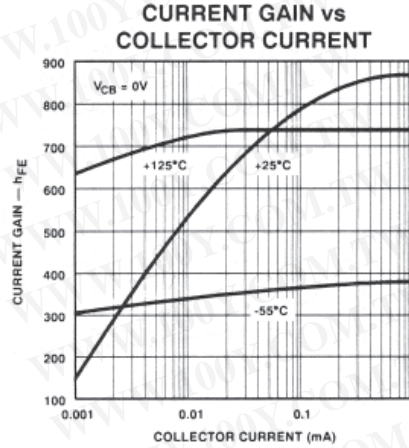
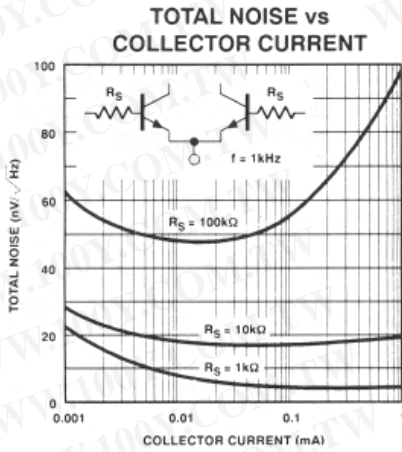
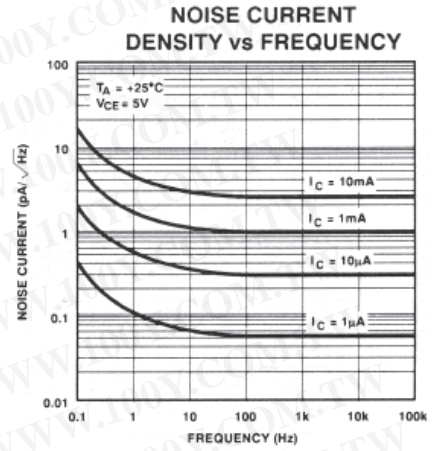
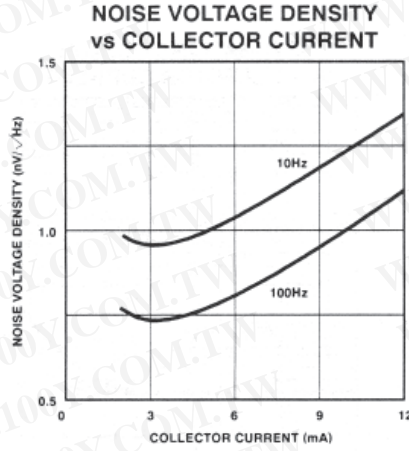
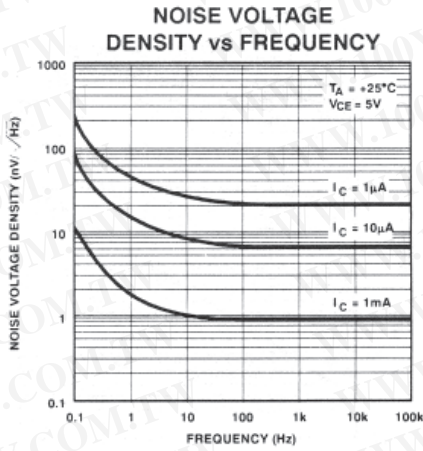


### EMITTER-BASE LOG CONFORMITY



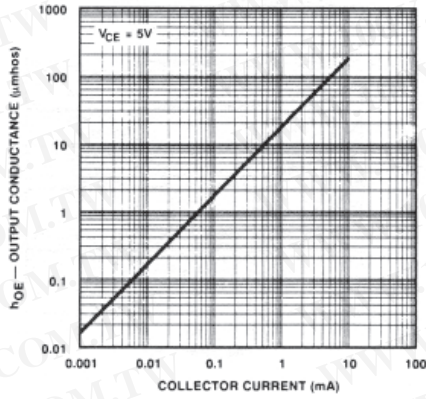
# SSM2210—Typical Performance Characteristics

## TYPICAL PERFORMANCE CHARACTERISTICS

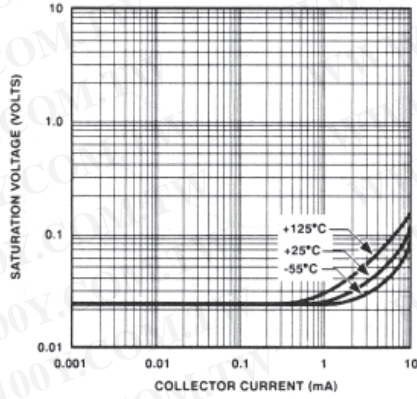


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

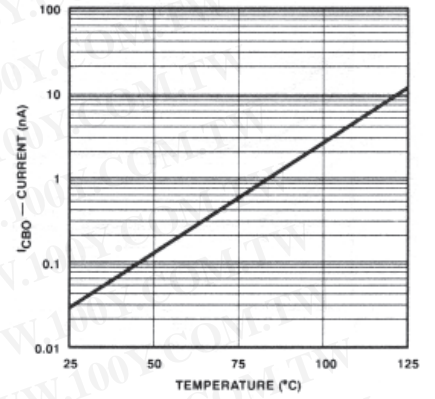
**SMALL-SIGNAL OUTPUT CONDUCTANCE vs COLLECTOR CURRENT**



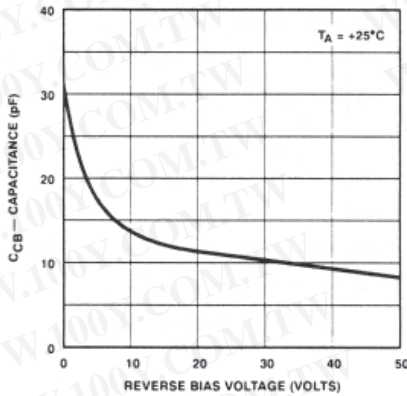
**SATURATION VOLTAGE vs COLLECTOR CURRENT**



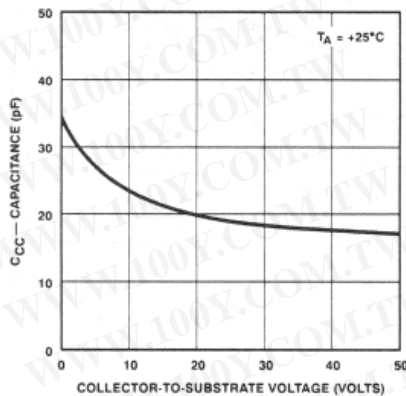
**COLLECTOR-TO-BASE LEAKAGE vs TEMPERATURE**



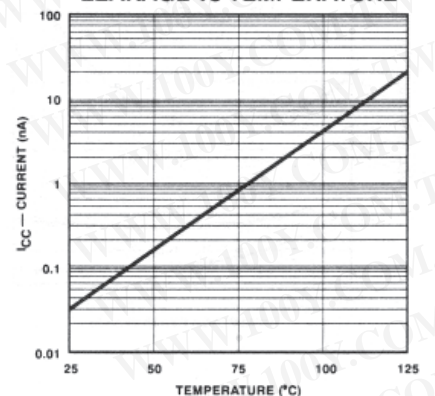
**COLLECTOR-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE**



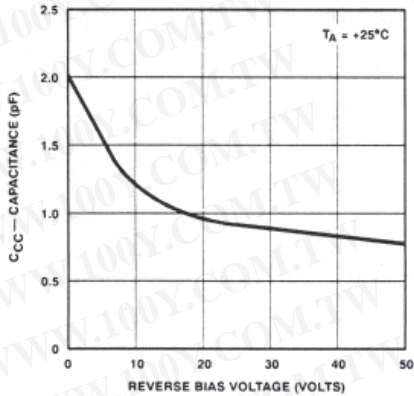
**COLLECTOR-TO-COLLECTOR CAPACITANCE vs COLLECTOR-TO-SUBSTRATE VOLTAGE**



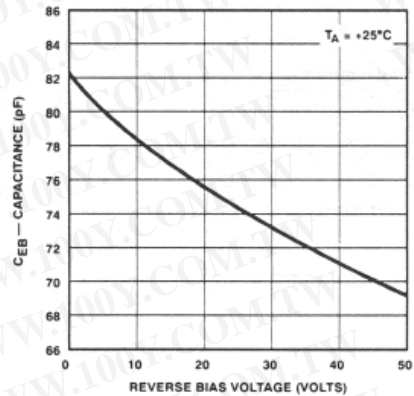
**COLLECTOR-TO-COLLECTOR LEAKAGE vs TEMPERATURE**



**COLLECTOR-TO-COLLECTOR CAPACITANCE vs REVERSE BIAS VOLTAGE**



**EMITTER-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE**



# SSM2210

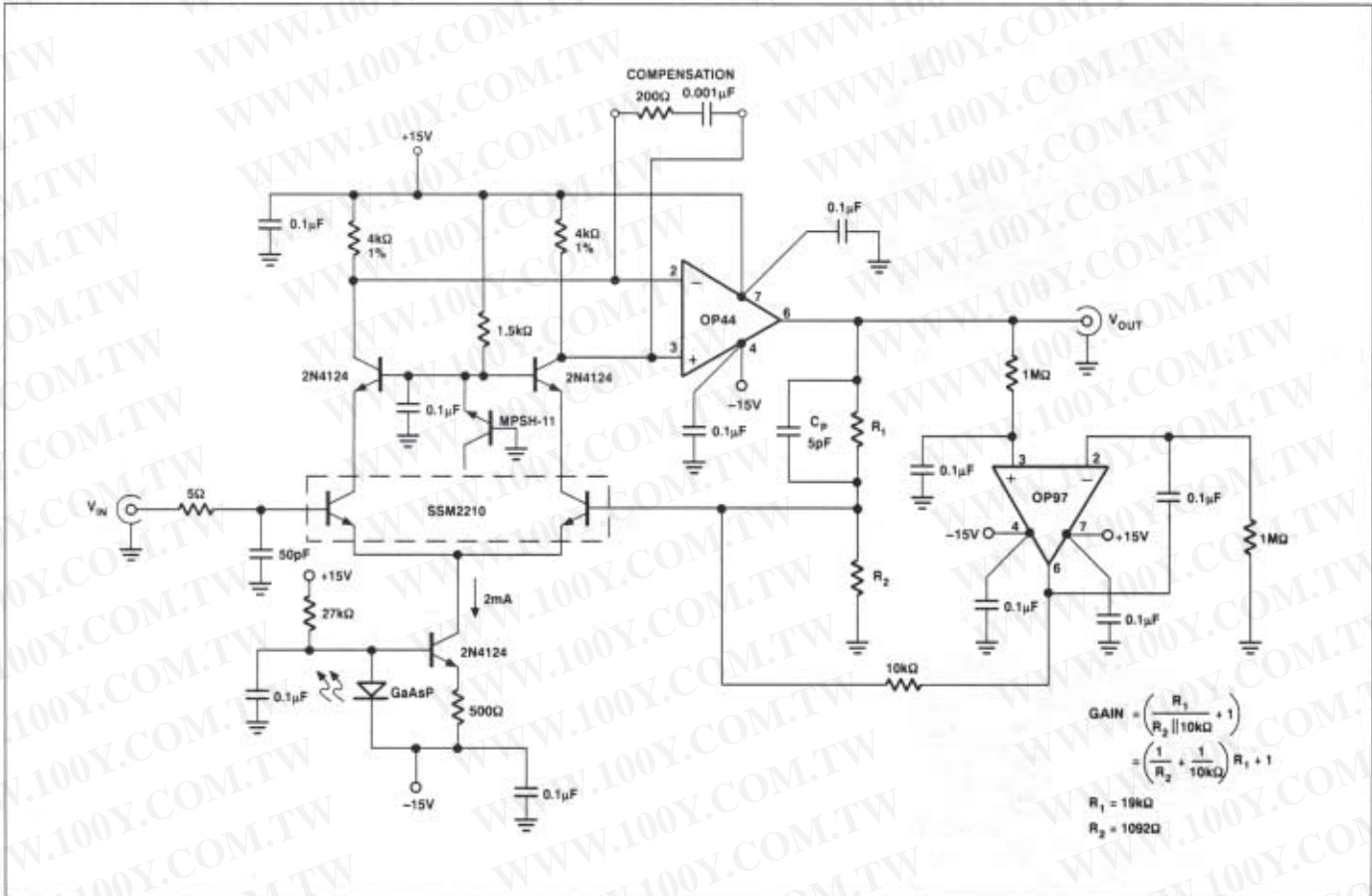


FIGURE 1: A Low-Noise Wideband Amplifier

## A VERY LOW-NOISE, WIDEBAND AMPLIFIER

Figure 1 illustrates a low-noise, wide-band amplifier consisting of a high slew rate JFET amplifier, the OP44, and a cascoded differential preamplifier using the SSM2210 transistor pair. The SSM2210 achieves extremely low input voltage noise performance ( $e_n \approx 0.7\text{nV}/\sqrt{\text{Hz}}$ ) via a large geometry transistor design which minimizes the base-spreading resistance. This, however, results in relatively higher collector-to-base capacitance ( $C_{OB}$ ) than ordinary small-signal transistors. For high gain stages, the Miller effect of  $C_{OB}$  will limit the voltage gain bandwidth; resorting to a cascode configuration reduces the Miller feedback capacitance, improving stability, bandwidth, and reducing distortion due to base-width modulation. Additionally, cascoding

does not increase the noise figure of the overall amplifier system and reduces the high order harmonic distortion.

The circuit in Figure 1 balances the impedance symmetrically in the differential preamp. This serves to reject common-mode noise injected from the power supplies.

Although the SSM2210's transistors are closely matched, an offset voltage error can still be created by imbalanced source impedances. Accordingly, a precision low-power amplifier (OP-97), configured as a noninverting integrator is implemented which servos-out the offset voltage to less than  $100\mu\text{V}$  referred to the input of the amplifier.

$$\text{GAIN} = \left( \frac{R_1}{R_2} + 1 \right)$$

$$= \left( \frac{1}{R_2} + \frac{1}{10\text{k}\Omega} \right) R_1 + 1$$

$$R_1 = 19\text{k}\Omega$$

$$R_2 = 1092\Omega$$

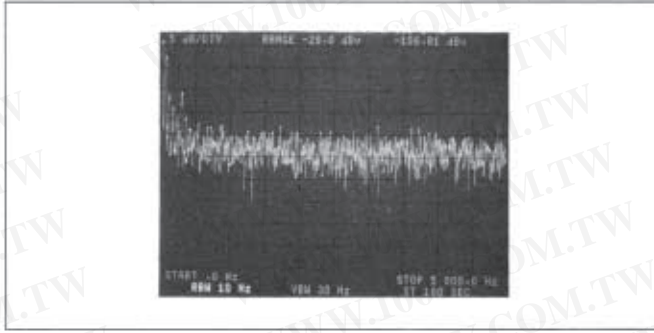


FIGURE 2: Spectrum Analyzer Display of Wideband Amplifier Noise Spectral Density.  $e_n \approx 1.7\text{nV}/\sqrt{\text{Hz}}$

Figure 2 illustrates the composite amplifier's low voltage noise density of only  $1.7\text{nV}/\sqrt{\text{Hz}}$  @ 1kHz. Figure 3 and Figure 4 show the excellent pulse response and an extremely low distortion of only 0.0015% over the audio bandwidth, respectively.

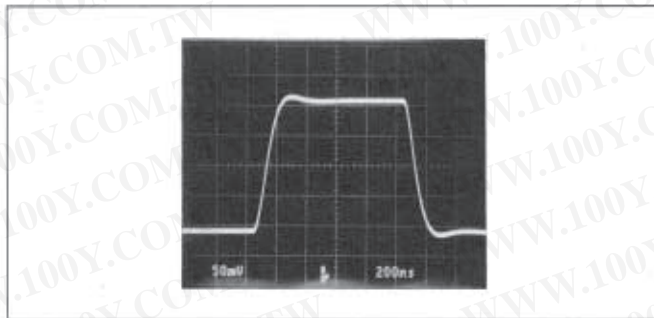


FIGURE 3: Small-Signal Pulse Response

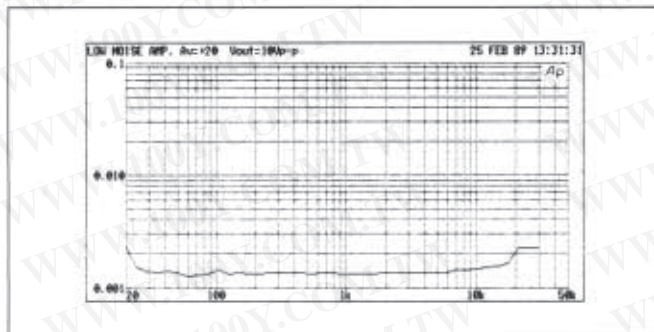


FIGURE 4: Total Harmonic Distortion vs Frequency

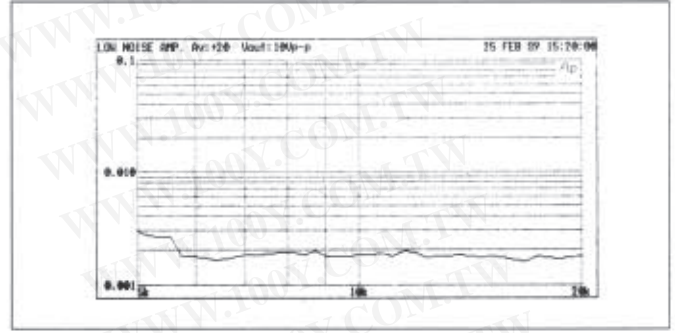


FIGURE 5: D.I.M. vs Frequency

A special test was performed to check for dynamic or transient intermodulation distortion. A square wave of 3.15kHz is mixed with a sine wave probe tone, and the resulting intermodulation distortion was found to be less than 0.002% (Figure 5). This is an impressively low value considering the amplifier's gain of 26dB. Interestingly, the GBW product of the composite amplifier was 63MHz which is much larger than that of the OP44 by itself. This is made possible by the SSM2210's cascaded preamplifier having a wide bandwidth and large signal gain.

The measured performance of this amplifier is summarized in Table 1.

TABLE 1: Measured Performance of the Low-Noise Wideband Amplifier

Slew-Rate	40V/ $\mu\text{s}$
Gain-Bandwidth	63.6 MHz
Input Noise Voltage Density @ 1kHz	1.7nV/ $\sqrt{\text{Hz}}$
Output Voltage Swing	$\pm 13\text{V}$
Input Offset Voltage	10 $\mu\text{V}$

# SSM2210

## 500pV/√Hz AMPLIFIER

In situations where low output, low-impedance transducers are used, amplifiers must have very low voltage noise to maintain a good signal-to-noise ratio. The design presented in this application is an operational amplifier with only 500pV/√Hz of broadband noise. The front end uses SSM2210 low-noise dual transistors to achieve this exceptional performance. The op amp has superb DC specifications compatible with high-precision transducer requirements, and AC specifications suitable for professional audio work.

### PRINCIPLE OF OPERATION

The design configuration in Figure 6 uses an OP27 op amp (already a low-noise design) preceded by an amplifier consisting of three parallel-connected SSM2210 dual transistors. Base spreading resistance (r<sub>bb</sub>) generates thermal noise which is reduced by a factor of √3 when the input transistors are parallel connected. Schottky noise, the other major noise-generating mechanism, is minimized by using a relatively high collector current (1mA per device). High current ensures a low dynamic emitter resistance, but does increase the base current and its associated current noise. Higher current noise is relatively unimportant when low-impedance transducers are used.

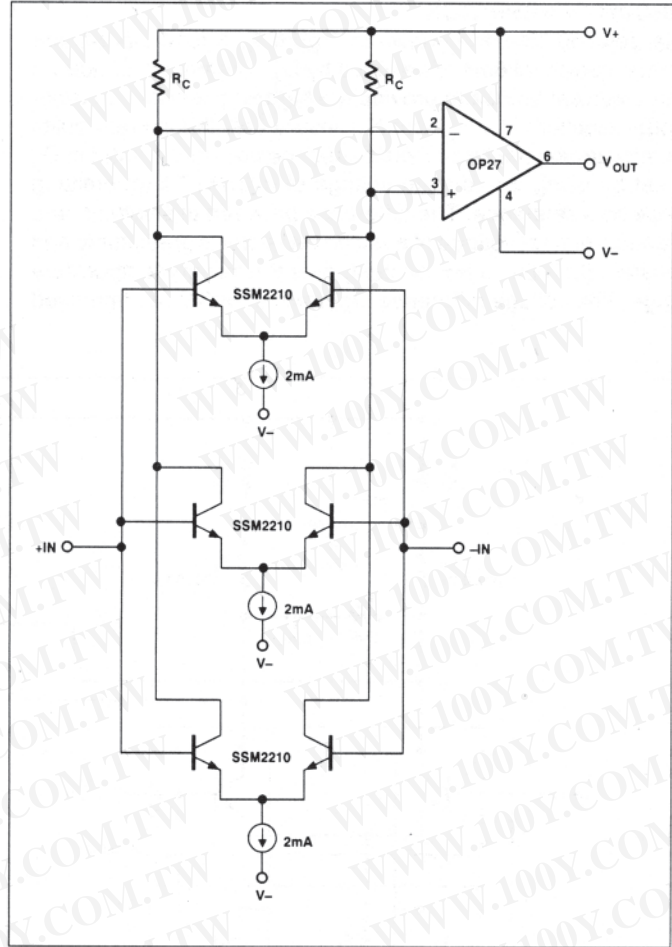


FIGURE 6: Simplified Schematic



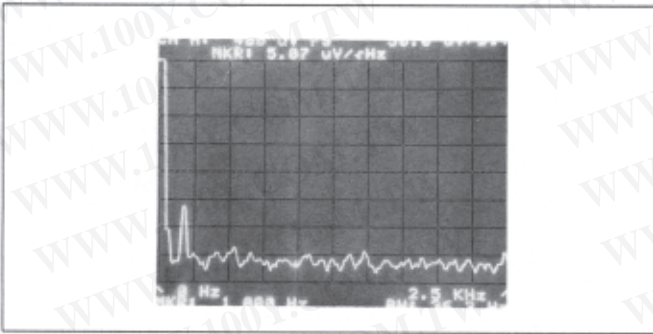
# SSM2210

## AMPLIFIER PERFORMANCE

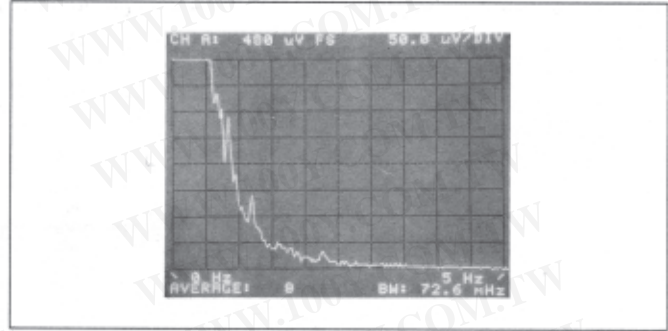
The measured performance of the op amp is summarized in Table 2. Figure 8 shows the broadband noise spectrum which is flat at about 500pV/√Hz. Figure 9 shows the low-frequency spectrum which illustrates the low 1/f noise corner at 1.5Hz. The low-frequency characteristic in the time domain from 0.1Hz to 10Hz is shown in Figure 10; peak-to-peak amplitude is less than 40nV.

**TABLE 2: Measured Performance of the Op Amp**

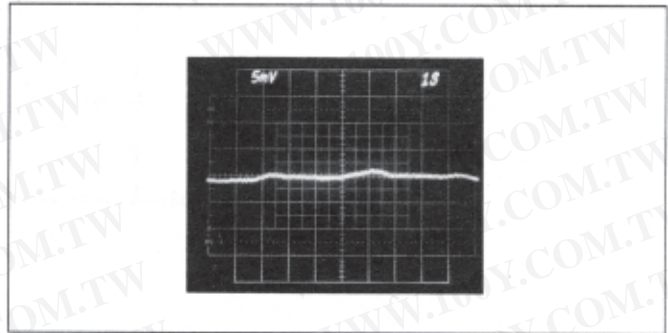
Input Noise		
Voltage Density at 1kHz		500pV/√Hz
Input Noise		
Voltage from 0.1Hz to 10Hz		40nV <sub>p-p</sub>
Input Noise Current at 1kHz		1.5pA/√Hz
Gain-Bandwidth	G = 10	3MHz
	G = 100	600kHz
	G = 1000	150kHz
Slew Rate		2V/μs
Open-Loop Gain		3 x 10 <sup>7</sup>
Common-Mode Rejection		130dB
Input Bias Current		3μA
Supply Current		10mA
Nulled TC <sub>V<sub>OS</sub></sub>		0.1μV/°C Max
T.H.D. at 1kHz	G = 1000	0.002%



**FIGURE 8: Spectrum Analyzer Display – Broadband**



**FIGURE 9: Spectrum Analyzer Display – Low Frequency**



**FIGURE 10: Oscilloscope Display**

## CONCLUSION

Using SSM2210 matched transistor pairs operating at a high current level, it is possible to construct a high-performance, low-noise operational amplifier. The circuit uses a minimum of components and achieves performance levels exceeding monolithic amplifiers.

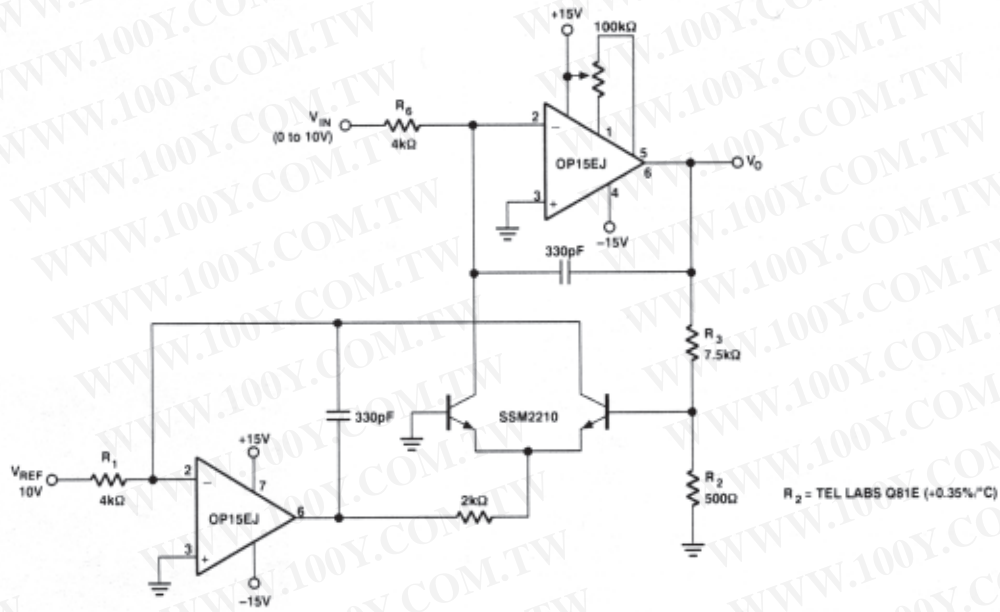


FIGURE 11: Fast Logarithmic Amplifier

### FAST LOGARITHMIC AMPLIFIER

The circuit of Figure 11 is a modification of a standard logarithmic amplifier configuration. Running the SSM2210 at 2.5mA per side (full-scale) allows a fast response with wide dynamic range. The circuit has a 7 decade current range, a 5 decade voltage range, and is capable of 2.5 $\mu$ s settling time to 1% with a 1 to 10V step.

The output follows the equation:

$$V_O = \frac{R_3 + R_2}{R_2} \frac{kT}{q} \ln \frac{V_{REF}}{V_{IN}}$$

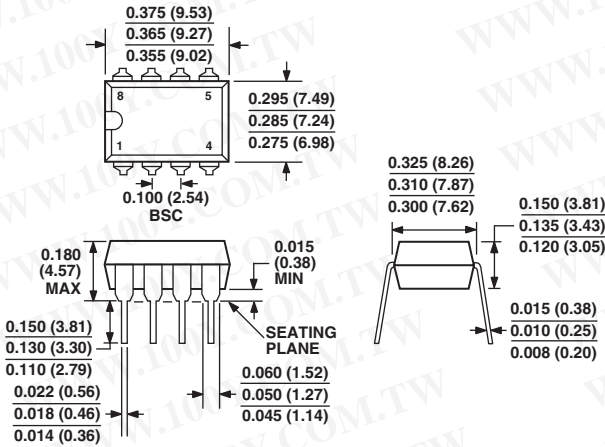
To compensate for the temperature dependence of the  $kT/q$  term, a resistor with a positive 0.35%/°C temperature coefficient is chosen for  $R_2$ .

The output is inverted with respect to the input, and is nominally -1V/decade using the component values indicated.

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]  
 [P-Suffix]  
 (N-8)

Dimensions shown in inches and (millimeters)

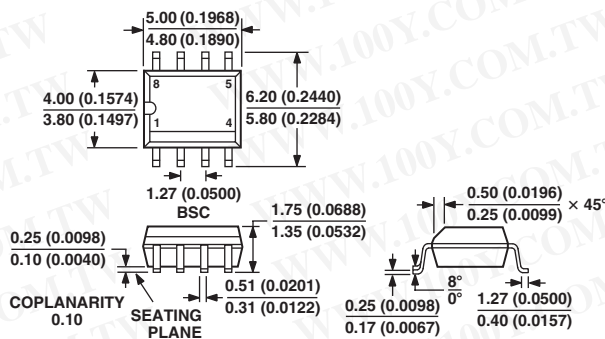


COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC]  
 Narrow Body  
 [S-Suffix]  
 (R-8)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

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