

Verilog2001 及 SystemVerilog 入門指引

■ 內容簡介

電路設計小型化和系統化是未來的趨勢，傳統電路層級的設計已不能滿足複雜化和小型化的要求，新一代的 **SystemVerilog** 一經提出，便已受到廣大的關注，在短短的幾年內，便得到所有 EDA 大場的全力支持，而且也得到 IEEE 認可為新的標準，做為 IC 設計的第二大國，我們不能忽視這個潮流。藉由本書大量的範例，可增加演練的機會，相信一定能提升電路設計的能力。本書適用於私立大學、科大電子、電機、資工系「硬體描述語言」並且使用 Verilog 之課程使用。

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